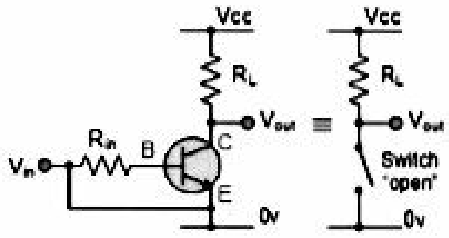


Transistor as a Switch

Transistor switches can be used to switch a low voltage DC device (e.g. LED's) ON or OFF by using a transistor in its saturated or cut-off state

When used as an AC signal amplifier, the transistors Base biasing voltage is applied in such a way that it always operates within its "active" region, that is the linear part of the output characteristics curves are used.

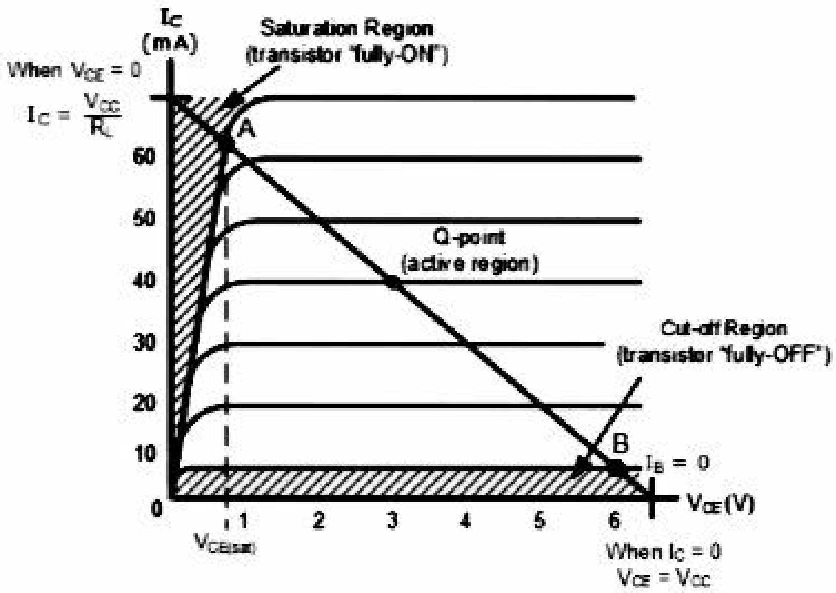
However, both the NPN & PNP type bipolar transistors can be made to operate as "ON/OFF" type solid state switch by biasing the transistors Base terminal differently to that for a signal amplifier.

Solid state switches are one of the main applications for the use of transistor to switch a DC output "ON" or "OFF". Some output devices, such as LED's only require a few milliamps at logic level DC voltages and can therefore be driven directly by the output of a logic gate. However, high power devices such as motors, solenoids or lamps, often require more power than that supplied by an ordinary logic gate so transistor switches are used.

If the circuit uses the **Bipolar Transistor as a Switch**, then the biasing of the transistor, either NPN or PNP is arranged to operate the transistor at both sides of the " I-V " characteristics curves we have seen previously.

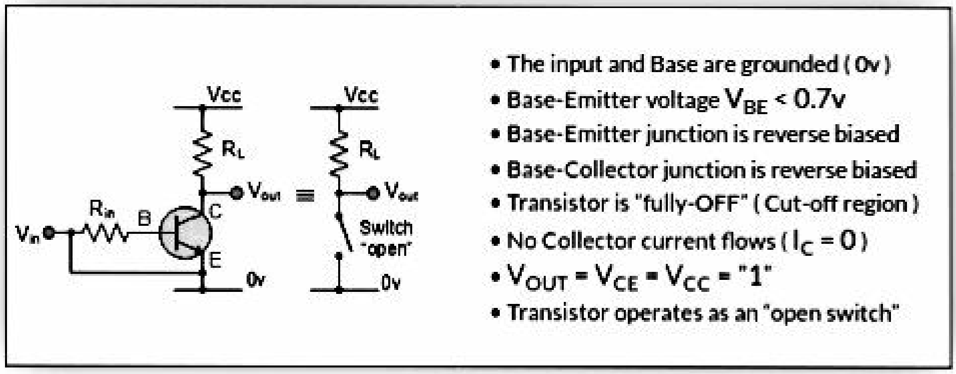
The areas of operation for a transistor switch are known as **the Saturation Region** and the **Cut-off Region**. This means then that we can ignore the operating Q-point biasing and voltage divider circuitry required for amplification, and use the transistor as a switch by driving it back and forth between its "fully-OFF" (cut-off) and "fully-ON" (saturation) regions as shown below.

Operating Regions



The pink shaded area at the bottom of the curves represents the "Cut-off" region while the blue area to the left represents the "Saturation" region of the transistor. Both these transistor regions are defined as:

Cut-off Characteristics

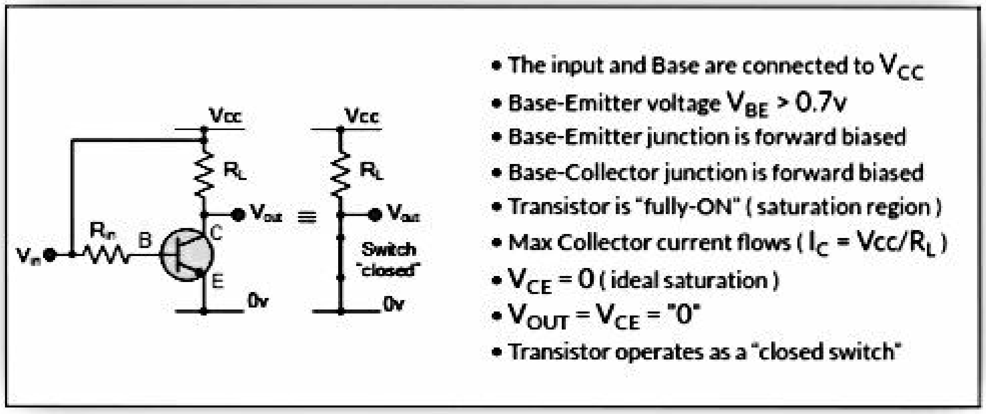


Then we can define the "cut-off region" or "OFF mode" when using a bipolar transistor as a switch as being, both junctions reverse biased, $V_B < 0.7v$ and $I_C = 0$. For a PNP transistor, the Emitter potential must be negative with respect to the Base.

2. Saturation Region

Here the transistor will be biased so that the maximum amount of base current is applied, resulting in maximum collector current resulting in the minimum collector emitter voltage drop which results in the depletion layer being as small as possible and maximum current flowing through the transistor. Therefore the transistor is switched "Fully-ON".

Saturation Characteristics



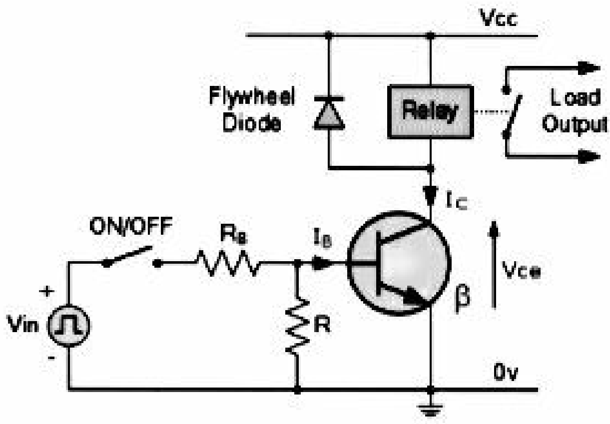
Then we can define the "saturation region" or "ON mode" when using a bipolar transistor as a switch as being, both junctions forward biased, $V_B > 0.7v$ and I_C = Maximum. For a PNP transistor, the Emitter potential must be positive with respect to the Base.

Then the transistor operates as a "single-pole single-throw" (SPST) solid state switch. With a zero signal applied to the Base of the transistor it turns "OFF" acting like an open switch and zero collector current flows. With a positive signal applied to the Base of the transistor it turns "ON" acting like a closed switch and maximum circuit current flows through the device.

The simplest way to switch moderate to high amounts of power is to use the transistor with an open-collector output and the transistors Emitter terminal connected directly to ground. When used in this way, the transistors open collector output can thus "sink" an externally supplied voltage to ground thereby controlling any connected load.

An example of an NPN Transistor as a switch being used to operate a relay is given below. With inductive loads such as relays or solenoids a flywheel diode is placed across the load to dissipate the back EMF generated by the inductive load when the transistor switches "OFF" and so protect the transistor from damage. If the load is of a very high current or voltage nature, such as motors, heaters etc, then the load current can be controlled via a suitable relay as shown.

Basic NPN Transistor Switching Circuit



The circuit resembles that of the *Common Emitter* circuit we looked at in the previous tutorials. The difference this time is that to operate the transistor as a switch the transistor needs to be turned either fully "OFF" (cut-off) or fully "ON" (saturated). An ideal transistor switch would have infinite circuit resistance between the Collector and Emitter when turned "fully-OFF" resulting in zero current flowing through it and zero resistance between the Collector and Emitter when turned "fully-ON", resulting in maximum current flow.

In practice when the transistor is turned "OFF", small leakage currents flow through the transistor and when fully "ON" the device has a low resistance value causing a small saturation voltage (V_{CE}) across it. Even though the transistor is not a perfect switch, in both the cut-off and saturation regions the power dissipated by the transistor is at its minimum.

In order for the Base current to flow, the Base input terminal must be made more positive than the Emitter by increasing it above the 0.7 volts needed for a silicon device. By varying this Base-Emitter voltage V_{BE}, the Base current is also altered and which in turn controls the amount of Collector current flowing through the transistor as previously discussed.

When maximum Collector current flows the transistor is said to be **Saturated**. The value of the Base resistor determines how much input voltage is required and corresponding Base current to switch the transistor fully "ON".

Transistor as a Switch Example No1

Using the transistor values from the previous tutorials of: β = 200, Ic = 4mA and Ib = 20uA, find the value of the Base resistor (Rb) required to switch the load fully "ON" when the input terminal voltage exceeds 2.5v.

$$R_B = \frac{V_{in} - V_{BE}}{I_B} = \frac{2.5v - 0.7v}{20x10^{-6}} = 90k\Omega$$

The next lowest preferred value is: 82kΩ, this guarantees the transistor switch is always saturated.

IC 555 multivibrator circuits

Objectives:

To design and study the following circuits using IC 555:

I. An astable multivibrator
II. A monostable multivibrator
III. A bistable multivibrator

Overview:

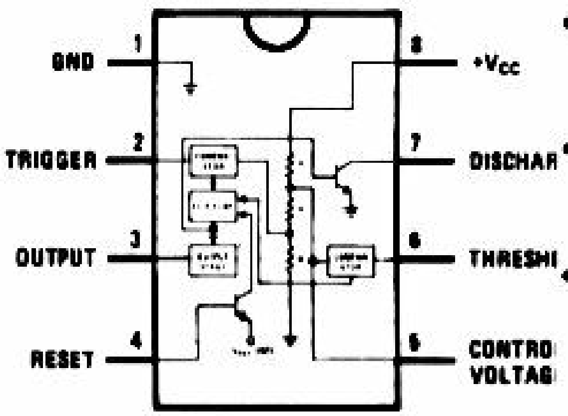
Multivibrators

Individual **Sequential Logic** circuits can be used to build more complex circuits such as Counters, Shift Registers, Latches or Memories etc, but for these types of circuits to operate in a "Sequential" way, they require the addition of a clock pulse or timing signal to cause them to change their state. **Clock pulses** are generally square shaped waves that are produced by a single pulse generator circuit such as a **Multivibrator** which oscillates between a "HIGH" and a "LOW" state and generally has an even 50% duty cycle, that is it has a 50% "ON" time and a 50% "OFF" time. Sequential logic circuits that use the clock signal for synchronization may also change their state on either the rising or falling edge, or both of the actual clock signal. There are basically three types of pulse generation circuits depending on the number of stable states,

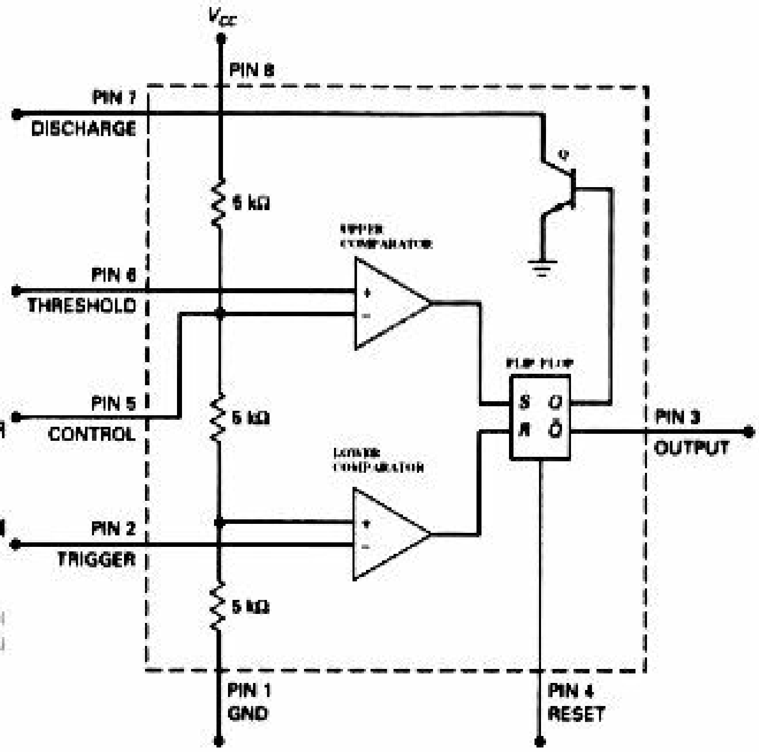
- Astable - has **NO** stable states but switches continuously between two states this action produces a train of square wave pulses at a fixed frequency.
- Monostable - has only **ONE** stable state and if triggered externally, it returns back to its first stable state.
- Bistable - has **TWO** stable states that produces a single pulse either positive or negative in value.

IC 555 TIMER

The 555 timer IC was first introduced around 1971 by the Signetics Corporation as the SE555/NE555 and was called "**The IC Time Machine**" and was also the very first and only commercial timer IC available. It provided circuit designers with a relatively cheap, stable, and user-friendly integrated circuit for timer and multivibrator applications. These ICs come in two packages, either the round metal-can called the 'T' package or the more familiar 8-pin DIP 'V' package as shown in figure below. The IC comprises of 23 transistors, 2 diodes and 16 resistors with built-in compensation for component tolerance and temperature drift.



IC 555 in 8-pin DIP package



Functional block diagram of IC 555

The pin connections are as follows:

1. Ground.
2. Trigger input.
3. Output.
4. Reset input.
5. Control voltage.
6. Threshold input.
7. Discharge.
8. $+V_{CC}$. +5 to +15 volts in normal use.

Pin1: Ground. All voltages are measured with respect to this terminal.

Pin2: Trigger. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. When a negative going pulse of amplitude greater than 1/3 V_{CC} is applied to this pin, the output of the timer high. The output remains high as long as the trigger terminal is held at a low voltage.

Pin3: Output. The output of the timer is measured here with respect to ground. There are two ways by which a load can be connected to the output terminal: either between pin 3 and ground or between pin3 and supply voltage $+V_{CC}$. When the output is low the load current flows through the load connected between pin3 and $+V_{CC}$ into the output terminal and is called sink current. The current through the grounded load is zero when the output is low. For this reason the load connected between pin 3 and $+V_{CC}$ is called the ***normally on load*** (we will use this for our circuit) and that connected between pin 3 and ground is called ***normally off-load***. On the other hand, when the output is high the current through the load connected between pin 3 and $+V_{CC}$ is zero. The output terminal supplies current to the normally off load. This current is called source current. The maximum value of sink or source current is 200mA.

Pin4: *Reset*. The 555 timer can be reset (*disabled*) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to $+V_{CC}$ to avoid any possibility of false triggering.

Pin5: *Control Voltage*. An external voltage applied to this terminal changes the threshold as well as trigger voltage. Thus by imposing a voltage on this pin or by connecting a *pot* between this pin and ground, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with a 0.01μF Capacitor to prevent any noise problems.

Pin6: *Threshold*. When the voltage at this pin is greater than or equal to the threshold voltage 2/3 V_{CC}, the output of the timer low.

Pin7: *Discharge*. This pin is connected internally to the collector of transistor Q. When the output is high Q is OFF and acts as an open circuit to external capacitor C connected across it. On the other hand, when the output is low, Q is saturated and acts as a short circuit, shorting out the external capacitor C to ground.

Pin8: $+V_{CC}$. The supply voltage of +5V to + 18V is applied to this pin with respect to ground.

OPERATION:

The functional block diagram shows that the device consists of two comparators, three resistors and a flip-flop. A comparator is an OPAMP that compares an input voltage and indicates whether an input is higher or lower than a reference voltage by swinging into saturation in both the direction. The operation of the 555 timer revolves around the three resistors that form a voltage divider across the power supply to develop the reference voltage, and the two comparators connected to this voltage divider. The IC is quiescent so long as the trigger input (pin 2) remains at $+V_{CC}$ and the threshold input (pin 6) is at ground. Assume the reset input (pin 4) is also at $+V_{CC}$ and therefore inactive, and that the control voltage input (pin 5) is unconnected.

The three resistors in the voltage divider all have the same value (5K in the bipolar version of this IC and hence the name 555), so the trigger and threshold comparator reference voltages are 1/3 and 2/3 of the supply voltage, respectively. The control voltage input at pin 5 can directly affect this relationship, although most of the time this pin is unused. The internal flip-flop changes state when the trigger input at pin 2 is pulled down below $+V_{CC}/3$. When this occurs, the output (pin 3) changes state to $+V_{CC}$ and the discharge transistor (pin 7) is turned off. The trigger input can now return to $+V_{CC}$; it will not affect the state of the IC.

However, if the threshold input (pin 6) is now raised above $+(2/3)V_{CC}$, the output will return to ground and the discharge transistor will be turned on again. When the threshold input returns to ground, the IC will remain in this state, which was the original state when we started this analysis. The easiest way to allow the threshold voltage (pin 6) to gradually rise to $+(2/3)V_{CC}$ is to connect it externally to a capacitor being allowed to charge through a resistor. In this way we can adjust the R and C values for almost any time interval we might want.

IC 555 Timer as Multivibrator

The 555 can operate in either mono/bi-stable or astable mode, depending on the connections to and the arrangement of the external components. Thus, it can either produce a single pulse when triggered, or it can produce a continuous pulse train as long as it remains powered.

Astable multivibrator

These circuits are not stable in any state and switch outputs after predetermined time periods. The result of this is that the output is a continuous square/rectangular wave with the properties depending on values of external resistors and capacitors. Thus, while designing these circuits following parameters need to be determined:

1. Frequency (or the time period) of the wave.
2. The duty cycle of the wave.

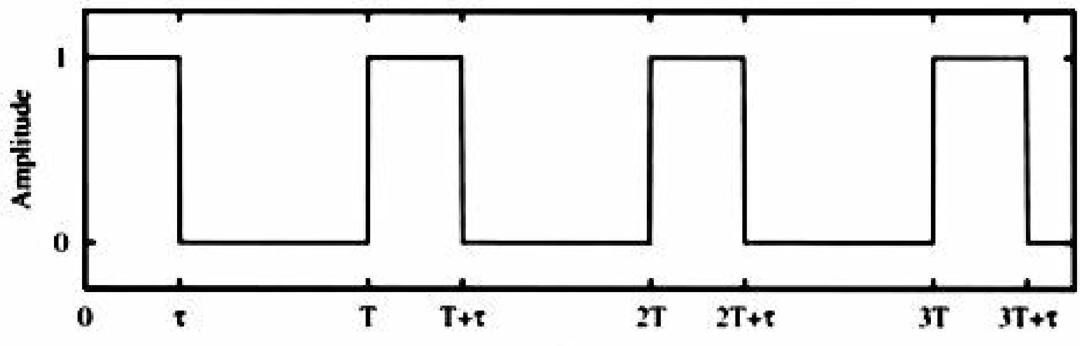


Figure 1: A rectangular waveform

Referring to the above figure of a rectangular waveform, the time period of the pulse is defined as T and duration of the pulse (ON time) is τ. Duty cycle can be defined as the On time/Period that is, τ/T in the above figure. Obviously, a duty cycle of 50% will yield a square wave.

The key external component of the **astable timer** is the *capacitor*. An astable multivibrator can be designed as shown in the circuit diagram (with typical component values) using IC 555, for a duty cycle of more than 50%. The corresponding voltage across the capacitor and voltage at output is also shown. The astable function is achieved by charging/discharging a capacitor through resistors connected, respectively, either to V_{CC} or GND. Switching between the charging and discharging modes is handled by resistor divider R1-R3, two Comparators, and an RS Flip-Flop in IC 555. **The upper or lower comparator** simply generates a positive pulse if V_C goes above 2/3 V_{CC} **or below** 1/3 V_{CC}. And these positive pulses either SET or RESET the Q output.

The time for charging C from 1/3 to 2/3 Vcc, i.e, **ON Time = 0.693 (R_A + R_B). C**
The time for discharging C from 2/3 to 1/3 Vcc, i.e. **OFF Time = 0.693 R_B. C**
To get the total oscillation period, just add the two:

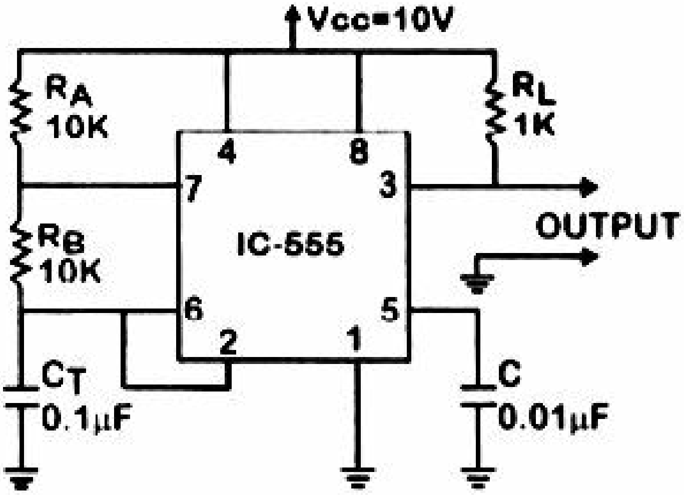
$$T_{osc} = 0.693 \cdot (R_A + R_B) \cdot C + 0.693 \cdot (R_B) \cdot C = 0.693 \cdot (R_A + 2 \cdot R_B) \cdot C$$

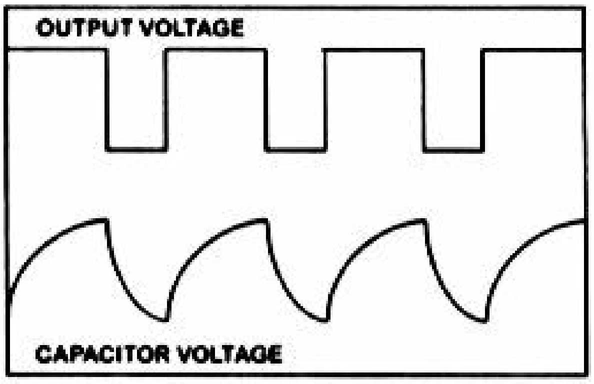
Thus,

$$f_{osc} = 1/T_{osc} = 1.44/(R_A + 2 \cdot R_B).C$$

$$\text{Duty cycle} = R_A + R_B / R_A + 2 \cdot R_B$$

Circuit Diagram:





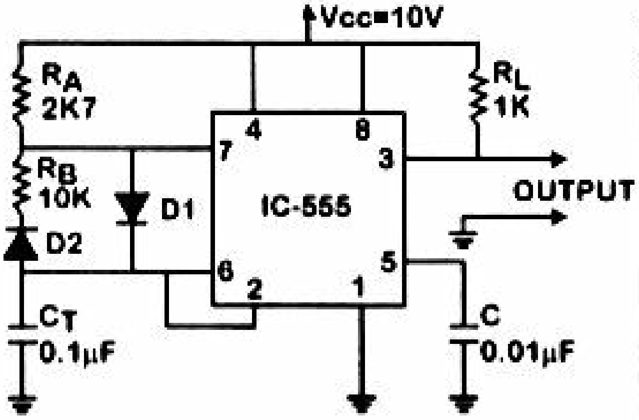
Astable multivibrator with duty cycle less than 50%:

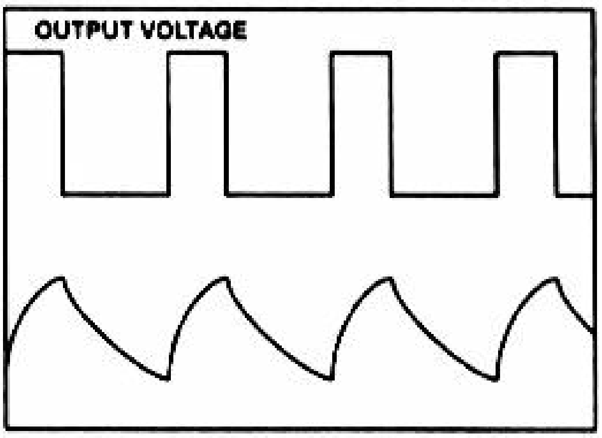
Generally astable mode of IC 555 is used to obtain the duty cycle between 50 to 100%. But for a duty cycle less than 50%, the circuit can be modified as per the circuit diagram. Here a diode D1 is connected between the discharge and threshold terminals (as also across R_B). Thus the capacitor now charges only through R_A (since R_B is shorted by diode conduction during charging) and discharges through R_B. Another optional diode D2 is also connected in series with R_B in reverse direction for better shorting of R_B. Therefore, the frequency of oscillation and duty cycle are

$$f_{osc} = 1/T_{osc} = 1.44/(R_A + R_B).C$$

$$\text{Duty Cycle} = R_A/(R_A + R_B)$$

Circuit Diagram:





Astable multivibrator with duty cycle variable from 0 to 100%:

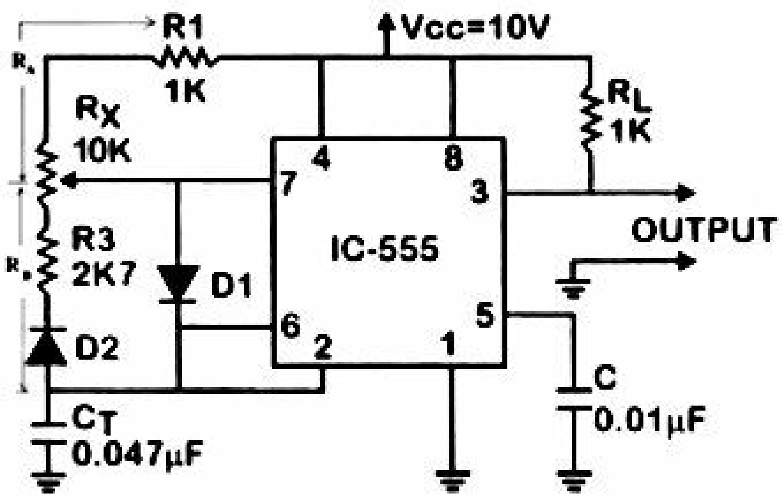
In some applications, it is needed to vary the duty cycle from about 0 to 100%. In that case the circuit is designed as shown in the circuit diagram. Here a potentiometer, R_X, is used so that $R_A = R_1+R_2$, $R_B = R_X-R_2+R_3$. A diode is now connected across a variable R_B. Thus a variable duty cycle is achieved. Therefore, the frequency of oscillation and duty cycle can be derived as follows.

$$f_{osc} = 1/T_{osc} = 1.44/(R_A + R_B).C = 1.44/(R_1 + R_X + R_3).C$$

$$\text{Min. Duty Cycle} = R_1/(R_1 + R_X + R_3)$$

$$\text{Max. Duty Cycle} = (R_1 + R_X)/(R_1 + R_X + R_3)$$

Circuit Diagram:



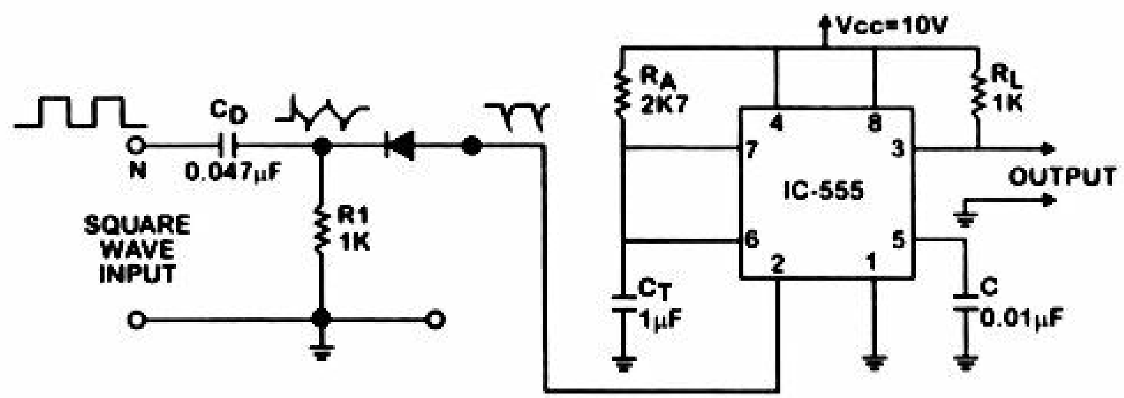
Monostable multivibrator

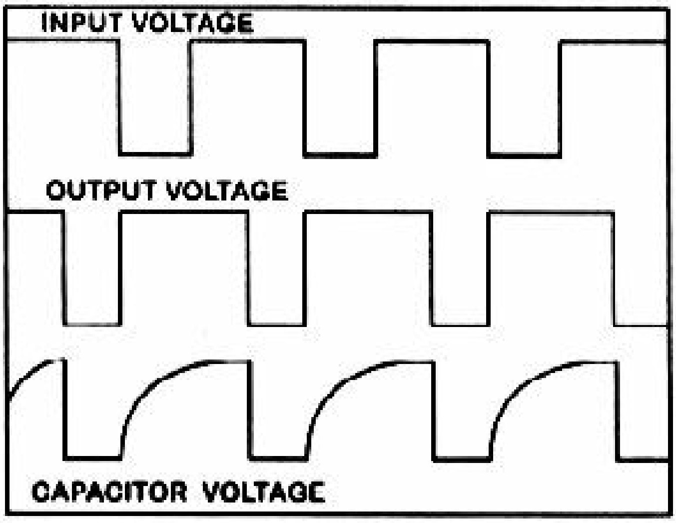
Monostable multivibrator often called a *one shot* multivibrator is a pulse generating circuit in which the duration of this pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby state, the output of the circuit is approximately zero or a logic-low level. When external trigger pulse is applied (See circuit diagram) output is forced to go high (= V_{CC}). The time for which output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until trigger pulse is again applied. Then the cycle repeats. The monostable circuit has only one stable state (*output low*) hence the name *monostable*.

Initially when the circuit is in the stable state i.e. when the output is low, transistor Q in IC 555 is ON and the capacitor C is shorted out to ground. Upon the application of a negative trigger pulse to pin 2, transistor Q is turned OFF, which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up towards V_{CC} through R. When the voltage across the capacitor equals 2/3 V_{CC}, the upper comparator's (see schematics of IC 555) output switches from low to high, which in turn drives the output to its low state via the output of the flip-flop. At the same time the output of the flip-flop turns transistor Q ON and hence the capacitor C rapidly discharges through the transistor. The output of the monostable remains low until a trigger pulse is again applied. Then the cycle repeats. The pulse width of the trigger input must be smaller than the expected pulse width of the output waveform. Also the trigger pulse must be a negative going input signal with amplitude larger than 1/3 V_{CC} (Why?). The pulse width can be calculated as (How?): **T= 1.1 R.C.**

Once triggered, the circuit's output will remain in the high state until the set time, T, elapses. The output will not change its state even if an input trigger is applied again during this time interval. The circuit can be reset during the timing cycle by applying negative pulse to the reset terminal. The output will remain in the low state until a trigger is again applied. The circuit is designed as shown in the circuit diagram, the left part of which shows how to generate negative a trigger pulse from a square wave signal.

Circuit Diagram:

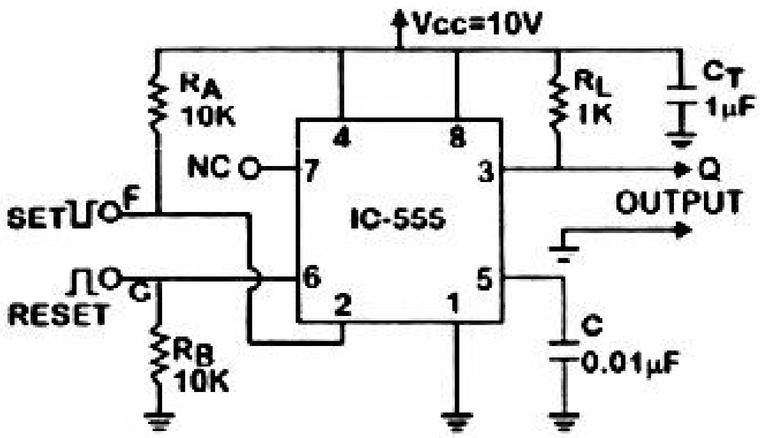




Bistable Multivibrator

In these circuits, the output is stable in both the states. The states are switched using an external trigger but unlike the monostable multivibrator, it does not return back to its original state. Another trigger is needed for this to happen. This operation is similar to a flip-flop. There are no RC timing network and hence no design parameters. The following circuit can be used to design a bistable multivibrator. The trigger and reset inputs (pins 2 and 4 respectively on a 555) are held high via pull-up resistors while the threshold input (pin 6) is simply grounded. Thus configured, pulling the trigger momentarily to ground acts as a 'set' and transitions the output pin (pin 3) to Vcc (high state). Pulling the threshold input to supply acts as a 'reset' and transitions the output pin to ground (low state). No capacitors are required in a bistable configuration.

Circuit Diagram:



Circuit components/Equipments:

1. IC 555 (1 No.)
2. Resistors (1KΩ, 2 Nos; 10KΩ, 2 Nos; 2.7KΩ, 1 No)
3. Potentiometer (10 KΩ, 1 No)
4. Capacitors (0.01 μF, 0.047 μF, 0.1 μF, 1 μF; 1 No. each)
5. Diodes IN 4148 (2 Nos.)
6. D.C. Power supply (10V)
7. Function Generators
8. Oscilloscope
9. Connecting wires
10. Breadboard

Circuit Diagrams: Already provided with text.

Procedure:

I. Astable Multivibrator:

(a) For duty cycle more than 50%:

1. Configure the circuit as per the circuit diagram.
2. Use $R_A = R_B = 10$ kΩ, $R_L = 1$ kΩ and $C_T = 0.1$ μF, $C = 0.01$ μF. Using the power supply set $V_{CC} = 10$ V.
3. Compute the expected values of f_{osc} and duty cycle (%).
4. Connect the output terminal (pin 3) to channel 1 of the oscilloscope. Also feed the voltage across capacitor to channel 2.
5. Power on your circuit and observe and save the output. Determine the values of f_{osc} and duty cycle (%) from your observations and compare with the theoretical values.
6. When you are done, turn off the power to your experimental circuit.

(b) For duty cycle less than 50%:

1. Configure the circuit as per the circuit diagram.
2. Use $R_A = 2.7$ kΩ, $R_B = 10$ kΩ, $R_L = 1$ kΩ and $C_T = 0.1$ μF, $C = 0.01$ μF. Using the power supply set $V_{CC} = 10$ V.
3. Repeat steps 3 to 6 of procedure (a).

(c) For duty cycle variable from 0 to 100%:

1. Configure the circuit as per the circuit diagram.
2. Use $R_1 = 1$ kΩ, $R_2 = 2.7$ kΩ, $R_X = 10$ kΩ, $R_L = 1$ kΩ and $C_T = 0.047$ μF, $C = 0.01$ μF. Using the power supply set $V_{CC} = 10$ V.
3. Calculate R_A and R_B for different settings of the potentiometer using $R_A = R_1+R_2$, $R_B = R_X-R_2+R_3$ and repeat steps 3 to 6 of procedure (a) for each setting.

II. Monostable Multivibrator

1. Configure the circuit as per the circuit diagram.

2. Use $\mathbf{R_1 = 1\ k\Omega}$, $\mathbf{R_A = 2.7\ k\Omega}$, $\mathbf{R_L = 1\ k\Omega}$ **and** $\mathbf{C_T = 1\ \mu F}$, $\mathbf{C_D = 0.047\ \mu F}$, $\mathbf{C = 0.01\ \mu F}$. Using the power supply set $\mathbf{V_{CC} = 10\ V}$.
3. Compute the expected value of pulse duration.
4. Apply a square wave input of frequency 1 kHz at terminal N of the circuit diagram.
5. Connect the output terminal (pin 3) to the oscilloscope. Also feed the voltage across capacitor to channel 2.
6. Power on your circuit and observe the output. Determine the value of pulse duration from your observations and compare with the theoretical values. Save the data.
7. When you are done, turn off the power to your experimental circuit.

III. Bistable Multivibrator

1. Configure the circuit as per the circuit diagram.
2. Use $\mathbf{R_A = R_B = 10\ k\Omega}$, $\mathbf{R_L = 1\ k\Omega}$ and $\mathbf{C_1 = 1\ \mu F}$, $\mathbf{C_2 = 0.01\ \mu F}$. Using the power supply set $\mathbf{V_{CC} = 10\ V}$.
3. Connect the output terminal (pin 3) to the oscilloscope in **DC COUPLING mode**.
4. Power on your circuit.
5. Connect the point F to ground momentarily. This will set the output Q in the oscilloscope to 1 or HIGH level. This state will be permanently stable state and the operation is called "SET".
6. Now connect the point G to V_{CC} momentarily. This will set the output Q in the oscilloscope to 0 or LOW level. This is called "RESET" operation.
7. When you are done, turn off the power to your experimental circuit

INTRODUCTION TO 555 TIMER IC

555 timer IC

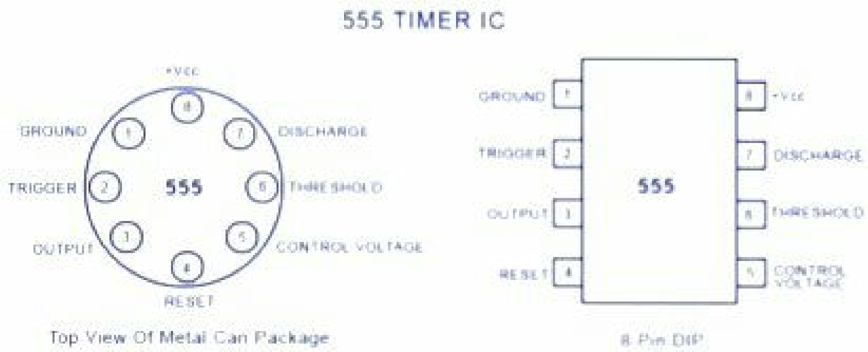
One of the most versatile linear ICs is the **555 timer** which was first introduced in early 1970 by Signetic Corporation giving the name as **SE/NE 555 timer**. This IC is a monolithic timing circuit that can produce accurate and highly stable time delays or oscillation. Like other commonly used op-amps, this IC is also very much reliable, easy to use and cheaper in cost. It has a variety of applications including **monostable** and **astable multivibrators**, **dc-dc converters**, digital logic probes, **waveform generators**, analog frequency meters and tachometers,**temperature measurement** and control devices, **voltage regulators** etc. The timer basically operates in one of the two modes either as a monostable (one-shot) multivibrator or as an astable (free-running) multivibrator.The **SE 555** is designed for the operating temperature range from – 55°C to 125° while the **NE 555**operates over a temperature range of 0° to 70°C.

The important features of the 555 timer are :

- It operates from a wide range of **power supplies** ranging from + 5 Volts to + 18 Volts supply voltage.
- Sinking or sourcing 200 mA of load current.
- The external components should be selected properly so that the timing intervals can be made into several minutes Proper selection of only a few external components allows timing intervals of several minutes along with the frequencies exceeding several hundred kilo hertz.
- It has a high current output; the output can drive TTL.

- It has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature, or equivalently 0.005 %/ °C.
- The duty cycle of the timer is adjustable with the maximum power dissipation per package is 600 mW and its trigger and reset inputs are logic compatible.

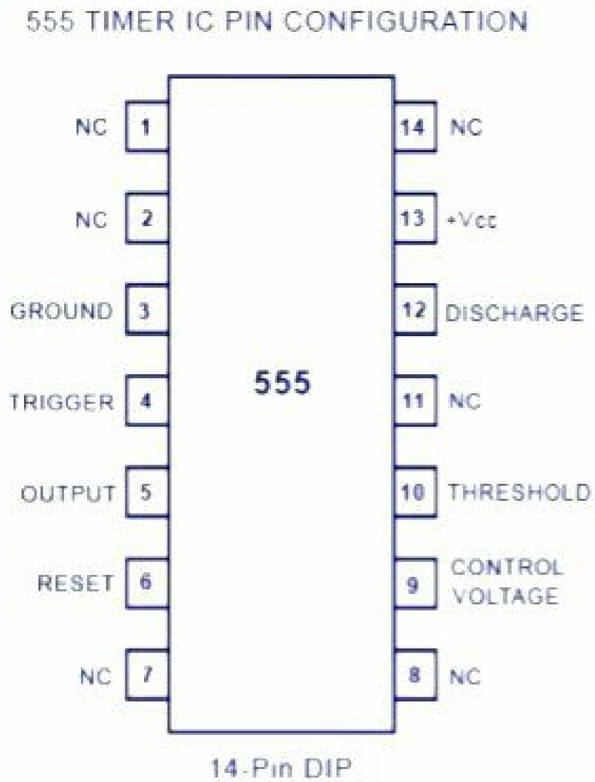
IC Pin Configuration



555 Timer IC Pin Configuration

The **555 Timer IC** is available as an 8-pin metal can, an 8-pin mini DIP (dual-in-package) or a 14-pin DIP.

This IC consists of 23 transistors, 2 diodes and 16 **resistors**. The explanation of terminals coming out of the 555 timer IC is as follows. The pin number used in the following discussion refers to the 8-pin DIP and 8-pin metal can packages.



Pin 1: **Grounded Terminal:** All the voltages are measured with respect to this terminal.

Pin 2: Trigger Terminal: This pin is an inverting input to a comparator that is responsible for transition of **flip-flop** from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin.

Pin 3: Output Terminal: Output of the timer is available at this pin. There are two ways in which a load can be connected to the output terminal either between pin 3 and ground pin (pin 1) or between pin 3 and supply pin (pin 8). The load connected between pin 3 and ground supply pin is called the ***normally on load***and that connected between pin 3 and ground pin is called the ***normally off load***.

Pin 4: Reset Terminal: To disable or reset the timer a negative pulse is applied to this pin due to which it is referred to as reset terminal. When this pin is not to be used for reset purpose, it should be connected to + V_{CC} to avoid any possibility of false triggering.

Pin 5: Control Voltage Terminal: The function of this terminal is to control the threshold and trigger levels. Thus either the external voltage or a pot connected to this pin determines the pulse width of the output waveform. The external voltage applied to this pin can also be used to modulate the output waveform. When this pin is not used, it should be connected to ground through a 0.01 micro Farad to avoid any noise problem.

Pin 6: **Threshold Terminal:** This is the non-inverting input terminal of comparator 1, which compares the voltage applied to the terminal with a reference voltage of 2/3 V_{CC}. The amplitude of voltage applied to this terminal is responsible for the set state of flip-flop.

Pin 7 : **Discharge Terminal:** This pin is connected internally to the collector of transistor and mostly a capacitor is connected between this terminal and ground. It is called discharge terminal because when transistor saturates, capacitor discharges through the transistor. When the transistor is cut-off, the capacitor charges at a rate determined by the external resistor and capacitor.

Pin 8: Supply Terminal: A supply voltage of + 5 V to + 18 V is applied to this terminal with respect to ground (pin 1).