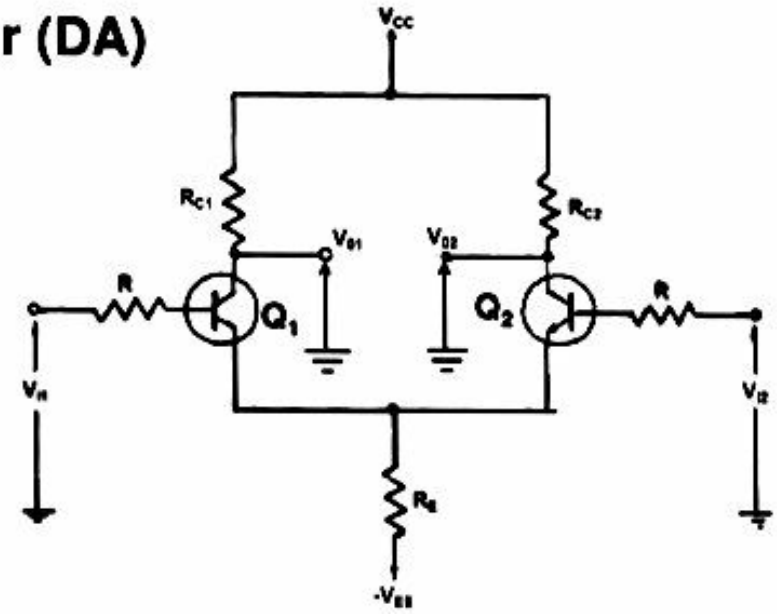
Differential amplifier (DA)

➢ A differential amplifier is a circuit that can accept two input signals and amplify the difference between these two input signals.

➢ Differential amplifier is a basic building block of an op-amp



The differential amplifier is a small signal amplifier. It is generally used as a voltage amplifier and not as current or power amplifier

Differential amplifier is a two input terminal device using at least two transistors. There are also two outputs terminals V_{o1} and V_{o2}.

Two transistor are matched so that they have identical characteristics. The collector resistance are also equal Rc1 = Rc2.

Differential amplifier

➢ Input signal can be applied by two ways –

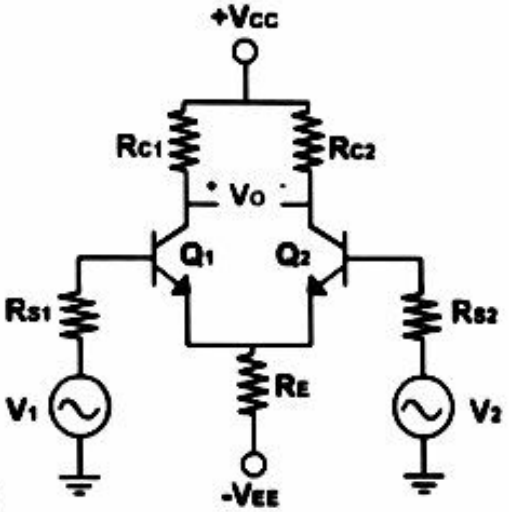
(a) Signal is applied to any one of the transistor and other input is grounded – single ended input arrangement

(b) Signals are applied to both the inputs of DA – double ended input arrangement

➢ Output signal can be taken from DA by two ways –

(a) Output signal is taken from any one of the output terminals and other output is grounded – single ended output arrangement

(b) Output signal is taken between two output terminals (between the collectors of Q1 and Q2) – double ended input arrangement



Generally Op-Amp is double ended input and single ended output device.

Operation of differential amplifier

- Suppose signal is applied to input 1 (the base of transistor Q1) and input 2 is grounded.
- Output of Q1 can be taken either at collector C (Q1 will act as a CE configuration) or emitter E (Q1 will work as a CC configuration).
- Output signal will be inverted and amplified at collector C of Q1
- Output signal will be non-inverted and of same magnitude as input signal at emitter E of Q1.
- If the output of Q1 is taken at emitter E – then this output will act as a input signal for transistor Q2 and Q2 will work as a CB configuration. Output of Q2 (CB configuration) is obtained at collector of Q2 (this will also be output of DA) and output signal will be non-inverted amplified signal.

Operation of differential amplifier (DA)

- Since DA and Op-Amp both have single ended output and double ended input so we discuss operation of single ended output and double ended input device.

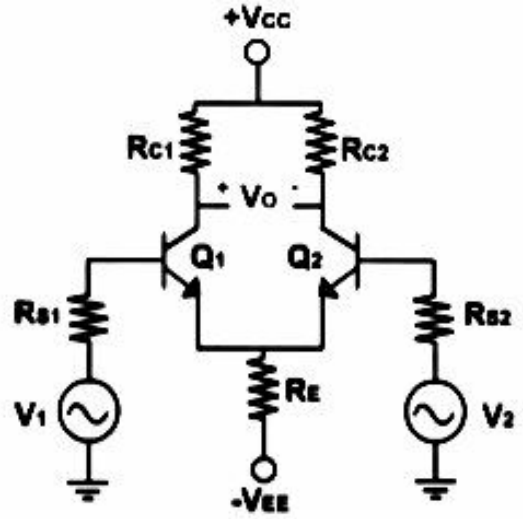
- Suppose output 2 is grounded and output of DA is taken at output 1. The input signal is applied either to input 1 or input 2 terminal.

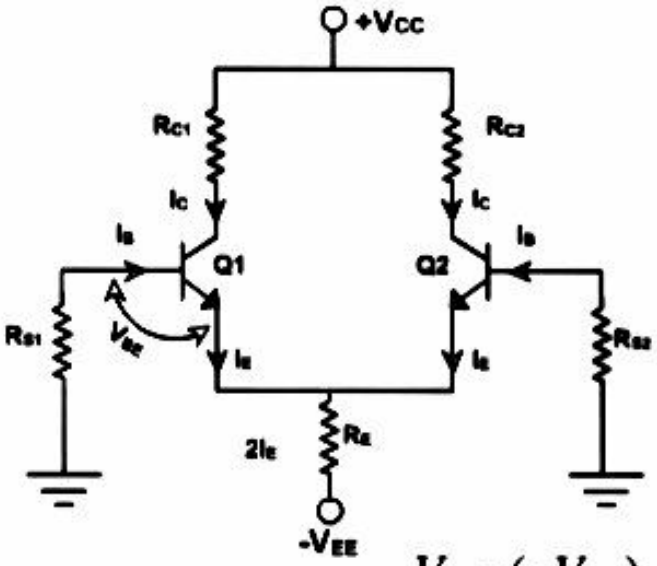
Input applied at	Output signal	Output taken at
Q1	Inverted amplified	Q1
Q2	Non-inverted amplified	Q1

- **If the signal applied to the input terminal results in opposite polarity output then input terminal is called inverting input, and if output is of same polarity as input then it is called non-inverting input.**

DC analysis of differential amplifier (DA)

Since both emitter biased sections of the DA are symmetrical in all respects, therefore, the operating point for only one section need to be determined.

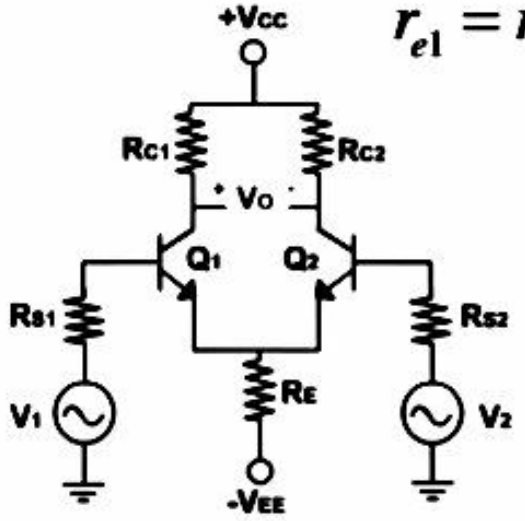




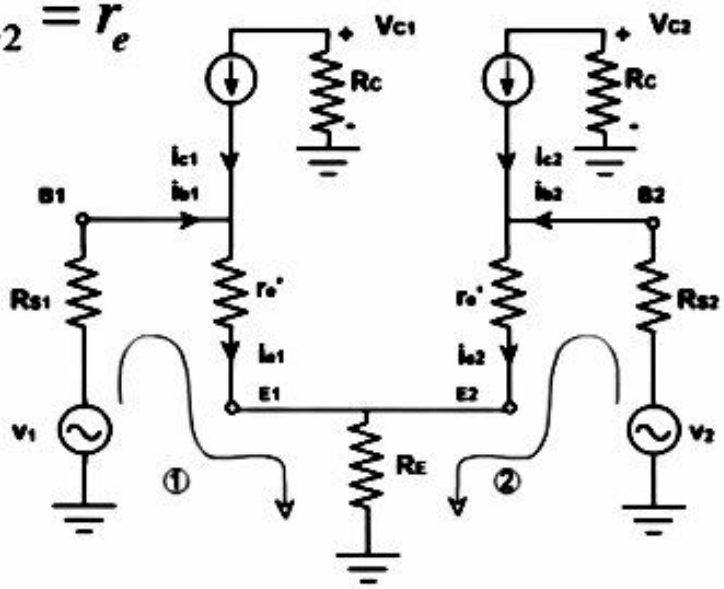
$$V_{BE} = V_B - V_E = 0.7; V_E = -0.7 \qquad I_E = \frac{V_E - (-V_{EE})}{2R_E}$$

$$\boxed{I_E = \frac{V_{EE} - 0.7}{2R_E}} \qquad I_{C1} = I_{C2} = I_E \qquad \boxed{V_{C1} = V_{CC} - I_{C1}R_{c1}}$$

AC analysis of differential amplifier (DA)



$$r_{e1} = r_{e2} = r_e$$



Applying KVL in two loops 1 & 2.

$$v_1 = R_{s1}i_{b1} + r_e i_{e1} + R_E(i_{e1} + i_{e2}) \qquad i_{b1} = i_{e1}/\beta$$

$$v_2 = R_{s2}i_{b2} + r_e i_{e2} + R_E(i_{e1} + i_{e2}) \qquad i_{b2} = i_{e2}/\beta$$

AC analysis of differential amplifier (DA)

Putting value of i_{b1} and i_{b2} and assuming R_{S1}/β and R_{S2}/β are very small in comparison with R_E and r_e' and therefore neglecting these terms,

$$v_1 = (r_e + R_E)i_{e1} + R_E i_{e2} \qquad v_2 = (r_e + R_E)i_{e2} + R_E i_{e1}$$

$$i_{e1} = \frac{(r_e + R_E)v_1 - R_E v_2}{(r_e + R_E)^2 - R_E^2} \qquad i_{e2} = \frac{(r_e + R_E)v_2 - R_E v_1}{(r_e + R_E)^2 - R_E^2}$$

The output voltage V_O is given by: $V_o = V_{c2} - V_{c1} = R_c(I_{c1} - i_{c2})$

$$v_o = R_C(i_{e1} - i_{e2}) = \frac{R_C}{r_e}(v_1 - v_2)$$

For Single ended input: $v_2 = 0$; therefore $I_{e1} = v_1 / 2r_e$ $\quad v_o = \frac{R_C}{2r_e}(v_1)$

Input & Output Resistance of DA

Differential input resistance is defined as the equivalent resistance that would be measured at either input terminal with the other terminal grounded. Resistance R_{S1} and R_{S2} are ignored because they are very small.

$$R_{i1} = \left(\frac{v_1}{i_{b1}}\right)_{v_2=0} = \frac{\beta v_1}{i_{e1}} \qquad i_{e1} = \frac{(r_e + R_E)v_1}{(r_e + R_E)^2 - R_E^2}$$

$$R_{i1} = \frac{\beta r_e(r_e + 2R_E)}{(r_e + R_E)}$$ **Since $R_E >> r_e$ hence** $R_{i1} = 2\beta \times r_e$

Output Resistance of DA

Output resistance is defined as the equivalent resistance that would be measured at output terminal with respect to ground. Therefore, the output resistance R_{O1} measured between collector C_1 and ground is equal to that of the collector resistance R_C. $R_{O1} = R_{O2} = R_C$

Common Mode Rejection Ratio (CMRR)

- If the signals v_{i1} and v_{i2} at the input terminals are opposite, the output voltage is highly amplified and if v_{i1} and v_{i2} are same, they are only slightly amplified.

- Overall operation : To amplify the difference signal while rejecting the common signal at the two inputs

- Noise is common to both inputs so the DA attenuates this input.

- Two signals v_{i1} and v_{i2} in general have both in-phase and out-of-phase components. So the resulting output $V_0 = A_d V_d + A_c V_c$

where A_d= Differential gain of the Amplifier
A_c = Common mode gain of the Amplifier
V_d= Difference voltage = $v_{i1} - v_{i2}$
V_c= Common voltage = = $(v_{i1} + v_{i2}) / 2$

Common Mode Rejection Ratio (CMRR)

CMRR is a measure of an amplifiers' ability to reject the common signals and defined as

$$\text{CMRR} = \frac{|A_d|}{|A_c|}$$

$$\text{or, } \text{CMRR(log)} = 20\log_{10}\frac{|A_d|}{|A_c|}$$

$$\text{Now, } v_o = A_d v_d + A_c v_c$$

$$= A_d v_d\left(1 + \frac{A_c v_c}{A_d v_d}\right) = A_d v_d\left(1 + \frac{A_c}{A_d}\frac{v_c}{v_d}\right)$$

$$= A_d v_d\left(1 + \frac{1}{\text{CMRR}}\frac{v_c}{v_d}\right)$$

The higher the CMRR , the better is DA.

Operational amplifier (OP-AMP)

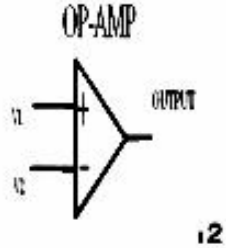
➢ An Op-Amp is a very high gain differential amplifier with very high input impedance (typically a few Mega ohm) and a low output impedance (less than 100Ω)

➢ Earlier, op-amp were used primarily to perform mathematical operation such as summation, subtraction, differentiation and integration etc. so named as op-amp.

➢ Typical application of op-amp includes – voltage amplitude change, oscillators, filter circuits and in instrumentation circuits.

➢ An Op-Amp have two inputs terminal called inverting (-ve terminal) and noninverting input (+ve terminal) and one output terminal.

➢ If the signal applied to the input terminal, results in opposite polarity output then input terminal is called inverting input, and if output is of same polarity input terminal is called non-inverting input.



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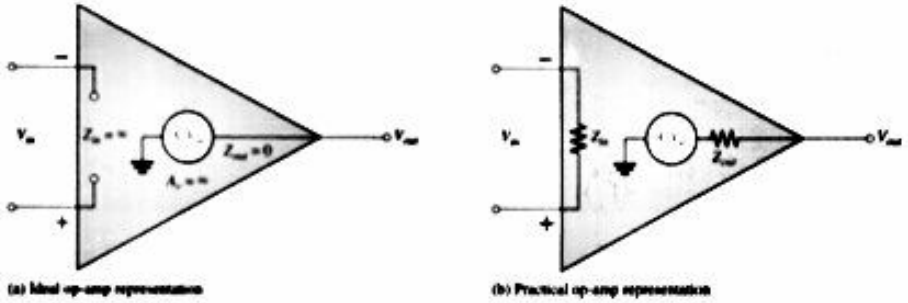
Characteristics of an Ideal Operational amplifier

Ideal op-amp has following characteristics -

- Input Resistance Ri= ∞
- Output Resistance Ro= 0
- Voltage Gain A = ∞
- Bandwidth = ∞
- Perfect balance i.e vo= 0 when v1= v2
- Characteristics do not drift with temperature



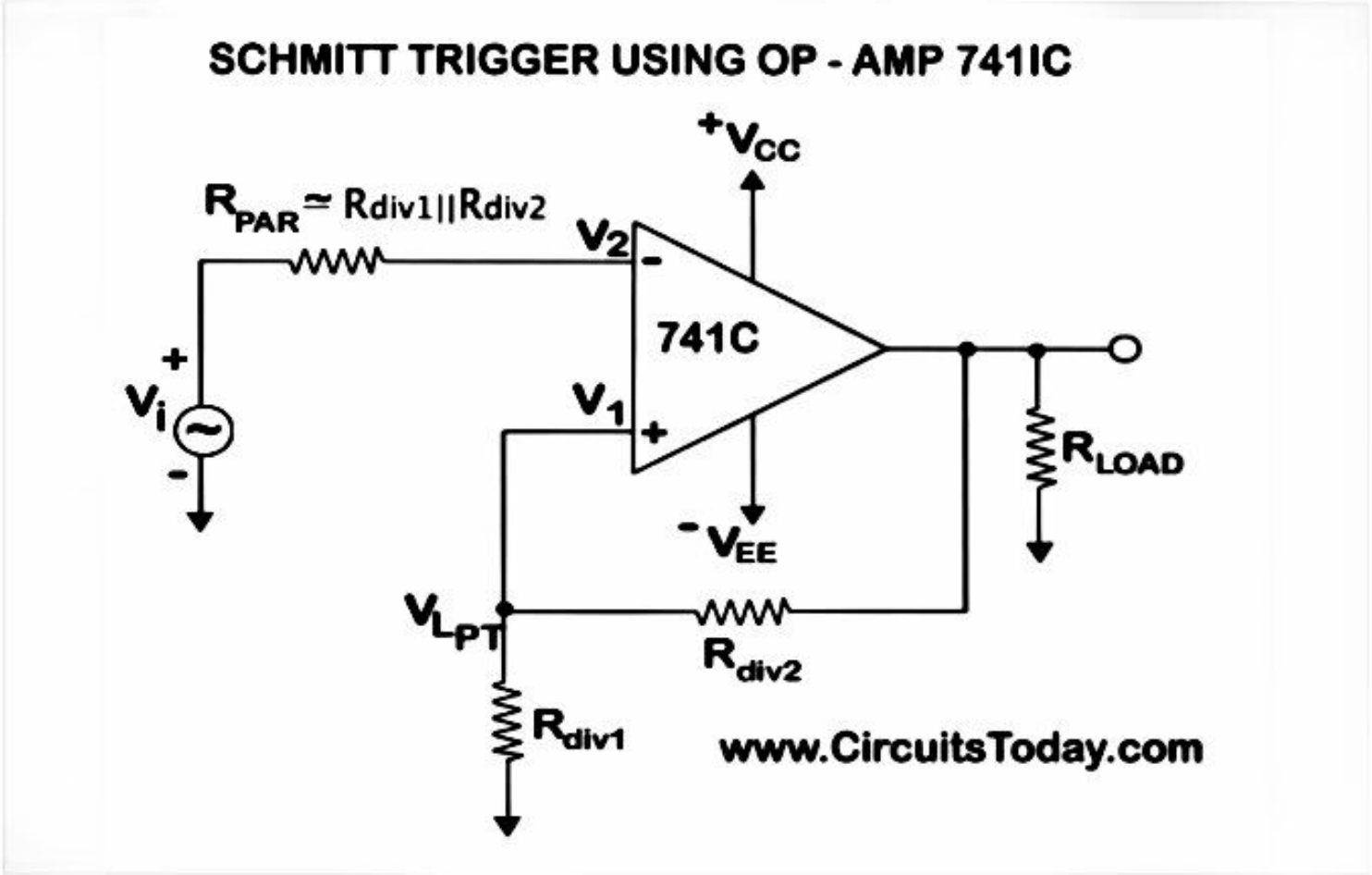
(a) Ideal op-amp representation

(b) Practical op-amp representation

SCHMITT TRIGGER USING OP-AMP

Schmitt Trigger or Regenerative Comparator Circuit

A Schmitt trigger circuit is also called a regenerative comparator circuit. The circuit is designed with a positive feedback and hence will have a regenerative action which will make the output switch levels. Also, the use of positive voltage feedback instead of a negative feedback, aids the feedback voltage to the input voltage, instead of opposing it. The use of a regenerative circuit is to remove the difficulties in a zero-crossing detector circuit due to low frequency signals and input noise voltages. Shown below is the circuit diagram of a Schmitt trigger. It is basically an inverting comparator circuit with a positive feedback. The purpose of the Schmitt trigger is to convert any regular or irregular shaped input waveform into a square wave output voltage or pulse. Thus, it can also be called a squaring circuit.

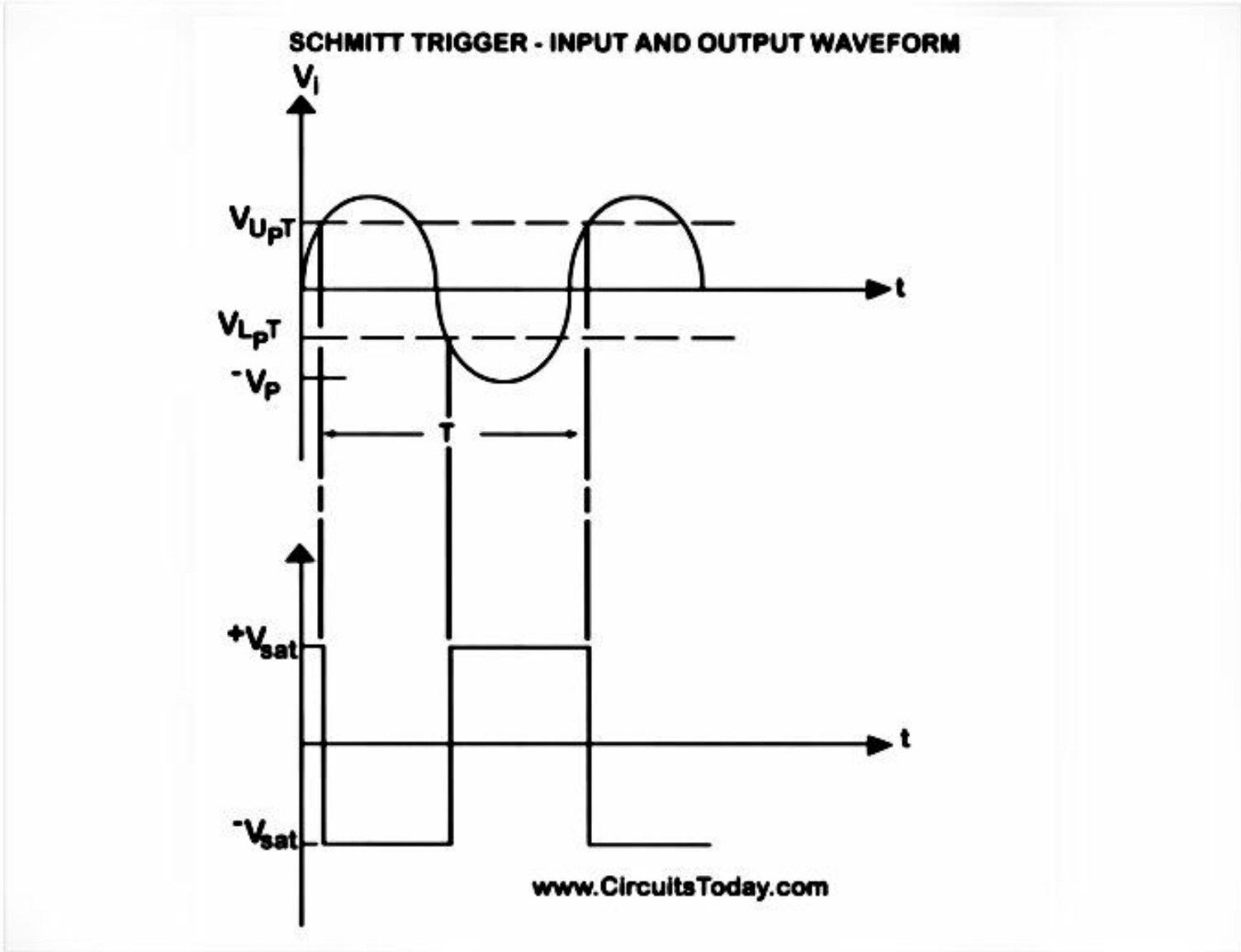


Schmitt Trigger Circuit Using Op-Amp uA741 IC

As shown in the circuit diagram, a voltage divider with resistors Rdiv1 and Rdiv2 is set in the positive feedback of the 741 IC op-amp. The same values of Rdiv1 and Rdiv2 are used to get the resistance value Rpar = Rdiv1||Rdiv2 which is connected in series with the input voltage. Rpar is used to minimize the offset problems. The voltage across R1 is fedback to the non-inverting input.

The input voltage Vi triggers or changes the state of output Vout every time it exceeds its voltage levels above a certain threshold value called Upper Threshold Voltage (Vupt) and Lower Threshold Voltage (Vlpt).

Let us assume that the inverting input voltage has a slight positive value. This will cause a negative value in the output. This negative voltage is fedback to the non-inverting terminal (+) of the op-amp through the voltage divider. Thus, the value of the negative voltage that is fedback to the positive terminal becomes higher. The value of the negative voltage becomes again higher until the circuit is driven into negative saturation (-Vsat). Now, let us assume that the inverting input voltage has a slight negative value. This will cause a positive value in the output. This positive voltage is fedback to the non-inverting terminal (+) of the op-amp through the voltage divider. Thus, the value of the positive voltage that is fedback to the positive terminal becomes higher. The value of the positive voltage becomes again higher until the circuit is driven into positive saturation (+Vsat). This is why the circuit is also named a regenerative comparator circuit.



Schmitt Trigger Input and Output Waveform

When Vout = +Vsat, the voltage across Rdiv1 is called Upper Threshold Voltage (Vupt). The input voltage, Vin must be slightly more positive than Vupt inorder to cause the output Vo to switch from +Vsat to -Vsat. When the input voltage is less than Vupt, the output voltage Vout is at +Vsat.

Upper Threshold Voltage, Vupt = +Vsat (Rdiv1/[Rdiv1+Rdiv2])

When Vout = -Vsat, the voltage across Rdiv1 is called Lower Threshold Voltage (Vlpt). The input voltage, Vin must be slightly more negaitive than Vlpt inorder to cause the output Vo to switch from -Vsat to +Vsat. When the input voltage is less than Vlpt, the output voltage Vout is at -Vsat.

Lower Threshold Voltage, Vlpt = -Vsat (Rdiv1/[Rdiv1+Rdiv2])

If the value of Vupt and Vlpt are higher than the input noise voltage, the positive feedback will eliminate the false output transitions. With the help of positive feedback and its regenerative behaviour, the output voltage will switch fast between the positive and negative saturation voltages.

Hysteresis Characteristics

Since a comparator circuit with a positive feedback is used, a dead band condition hysteresis can occur in the output. When the input of the comparator has a value higher than Vupt, its output switches from +Vsat to -Vsat and reverts back to its original state, +Vsat, when the input value goes below Vlpt. This is shown in the figure below. The hysteresis voltage can be calculated as the difference between the upper and lower threshold voltages.

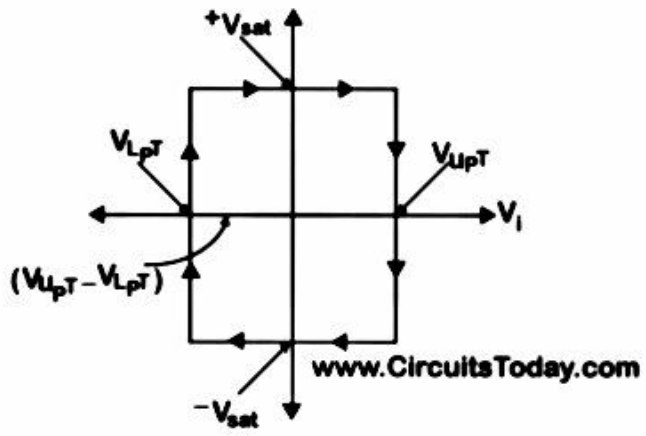
Vhysteresis = Vupt – Vlpt

Subsituting the values of Vupt and Vlpt from the above equations:

Vhysteresis = +Vsat (Rdiv1/Rdiv1+Rdiv2) – {-Vsat (Rdiv1/Rdiv1+Rdiv2)}

Vhysteresis = (Rdiv1/Rdiv1+Rdiv2) {+Vsat – (-Vsat)}

SCHMITT TRIGGER - INPUT OUTPUT CHARECTERISTICS-HYSTERISIS VOLTAGE PLOT



Schmitt-Trigger-Hysteresis Characteristics

Applications of Schmitt Trigger

Schmitt trigger is mostly used to convert a very slowly varying input voltage into an output having abruptly varying waveform occurring precisely at certain predetermined value of input voltage. Schmitt trigger may be used for all applications for which a general comparator is used. Any type of input voltage can be converted into its corresponding square signal wave. The only condition is that the input signal must have large enough excursion to carry the input voltage beyond the limits of the hysteresis range. The amplitude of the square wave is independent of the peak-to-peak value of the input waveform.

68.1 What is an OP-AMP ?

It is a very high-gain, high-r_{in} directly-coupled negative-feedback amplifier which can amplify signals having frequency ranging from **0 Hz to a little beyond 1 MHz.** They are made with different internal configurations in linear *ICs*. An *OP-AMP* is so named because it was originally designed to perform mathematical operations like summation, subtraction, multiplication, differentiation and integration etc. in analog computers. Present day usage is much wider in scope but the popular name *OP-AMP* continues.

Typical uses of *OP-AMP* are : scale changing, analog computer operations, in instrumentation and control systems and a great variety of phase-shift and oscillator circuits. The *OP-AMP* is available in three different packages (*i*) standard dual-in-line package (*DIL*) (*ii*) *TO*-5 case and (*iii*) the flat-pack.

Although an *OP-AMP* is a complete amplifier, it is so designed that external components (resistors, capacitors etc.) can be connected to its terminals to change its external characteristics. Hence, it is relatively easy to tailor this amplifier to fit a particular application and it is, in fact, due to this versatility that *OP-AMPs* have become so popular in industry.

An *OP-AMP IC* may contain two dozen transistors, a dozen resistors and one or two capacitors.

Example of OP-AMPs

1. μA 709—is a high-gain operational amplifier constructed on a single silicon chip using planar epitaxial process.

   It is intended for use in dc servo systems, high-impedance analog computers and in low-level instrumentation applications.

   It is manufactured by Semiconductors Limited, Pune.
2. [*LM* 108 – *LM* 208]— Manufactured by Semiconductors Ltd. Bombay,
3. *CA* 741 *CT* and *CA* 741 *T*—these are high-gain operational amplifiers which are intended for use as (*i*) comparator, (*ii*) integrator, (*iii*) differentiator, (*iv*) summer, (*v*) dc amplifier, (*vi*) multivibrator and (*vii*) bandpass filter.

   Manufactured by Bharat Electronics Ltd (*BEL*), Bangalore.

68.2. OP-AMP Symbol

Standard triangular symbol for an *OP-AMP* is shown in Fig. 68.1 (*a*) though the one shown in Fig. 68.1 (*b*) is also used often. In Fig. 68.1 (*b*), **the common ground line has been omitted.** It also does not show other necessary connections such as for dc power and feedback etc.

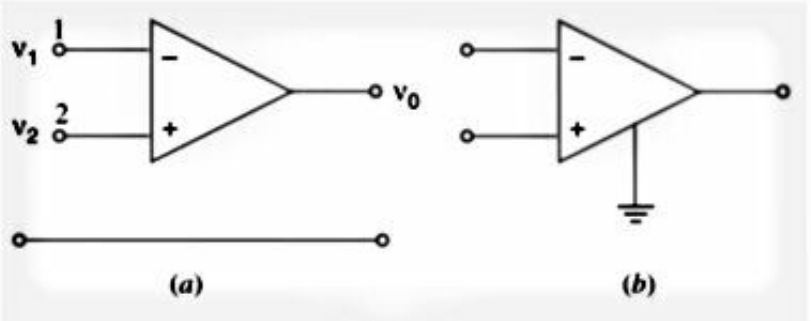


Fig. 68.1

The *OP-AMP's* input can be single-ended or double-ended (or differential input) depending on whether input voltage is applied to one input terminal only or to both. Similarly, amplifier's output can also be either single-ended or double-ended. The most common configuration is ***two input terminals and a single output.***

All OP-AMPs have a minimum of five terminals :

1. inverting input terminal,
2. non-inverting input terminal,
3. output terminal,
4. positive bias supply terminal,
5. negative bias supply terminal.

68.3. Polarity Conventions

In Fig. 68.1 (*b*), the input terminals have been marked with minus (–) and plus (+) signs. These are meant to **indicate the inverting and non-inverting terminals only** [Fig. 68.2]. It simply means that a signal applied at negative input terminal will appear amplified but **phase-inverted at the output terminal** as shown in Fig. 68.2 (*b*). Similarly, signal applied at the positive input terminal will appear amplified and **inphase** at the output. Obviously, these plus and minus polarities **indicate phase reversal only**. It does not mean that voltage v_1 and v_2 in Fig. 68.2 (*a*) are negative and positive respectively. Additionally, it also does not imply that a ***positive input voltage has to be connected to the plus-marked non-inverting terminal 2 and negative input voltage to the negative-marked inverting terminal 1.*** In fact, the amplifier can be used 'either way up' so to speak. It may also be noted that all input and output voltages are referred to a common reference usually the ground shown in Fig. 68.1 (*a*).

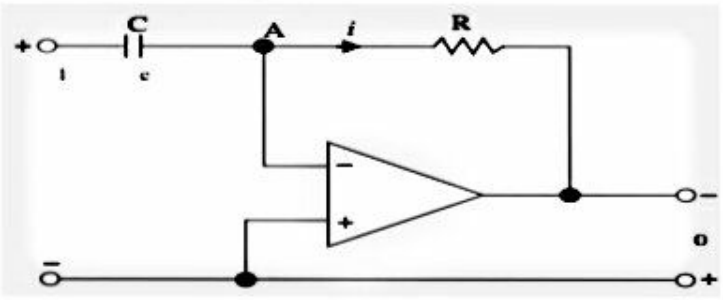


Fig. 68.2

68.4. Ideal Operational Amplifier

When an *OP-AMP* is operated without connecting any resistor or capacitor from its output to any one of its inputs (*i.e.*, without feedback), it is said to be in the **open-loop condition**. The word 'open loop' means that ***feedback path or loop is open***. The specifications of *OP-AMP* under such condition are called open-loop specifications.

An ideal *OP-AMP* (Fig. 68.3) has the following characteristics :

1. its open-loop gain A_v is ***infinite*** *i.e.*, $A_v = -\infty$
2. its input resistance R_i (measured between inverting and non-inverting terminals) is ***infinite*** *i.e.*, $R_i = \infty$ ohm
3. its output resistance R_0 (seen looking back into output terminals) is *zero i.e.*, $R_0 = 0\ \Omega$
4. it has ***infinite bandwith*** *i.e.*, it has flat frequency response from dc to infinity.

Though these characteristics cannot be achieved in practice, yet an ideal *OP-AMP* serves as a convenient reference against which real *OP-AMPs* may be evaluated.

Following additional points are worth noting :

1. infinte input resistance means that input current $i = 0$ as indicated in Fig. 68.3. It means that an ideal *OP-AMP* is a voltage-controlled device.
2. $R_0 = 0$ means that v_0 is not dependent on the load resistance connected across the output.
3. though for an ideal *OP-AMP* $A_v = \infty$, for an actual one, it is extremely high *i.e.*, about 10^6. However, it does not mean that 1 V signal will be amplified to 10^6 V at the output. Actually, the maximum value of v_0 is limited by the basis supply voltage, typically ± 15 V. With $A_v = 10^6$ and $v_0 = 15\ V_2$ the maximum value of input voltage is limited to $15/10^6 = 15\ \mu V$. Though 1 μV in the *OP-AMP*, can certainly become 1 V.

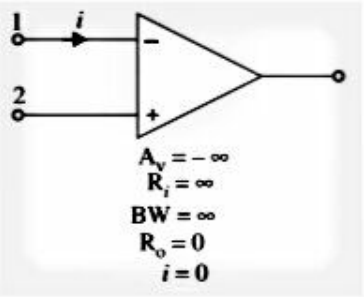


Fig. 68.3

68.5. Virtual Ground and Summing Point

In Fig. 68.4 is shown an *OP-AMP* which *employs negative feedback* with the help of resistor R_f which feeds a portion of the output to the input.

Since input and feedback currents are algebraically added at point *A*, it is called the **summing point.**

The concept of **virtual** ground arises from the fact that input voltage v_i at the inverting terminal of the *OP-AMP* is forced to such a small value that, for all practical purposes, it may be assumed to be zero. Hence, point *A* is essentially at ground voltage and is referred to as *virtual ground.* Obviously, ***it is not the actual ground,*** which, as seen from Fig. 68.4, is situated below.

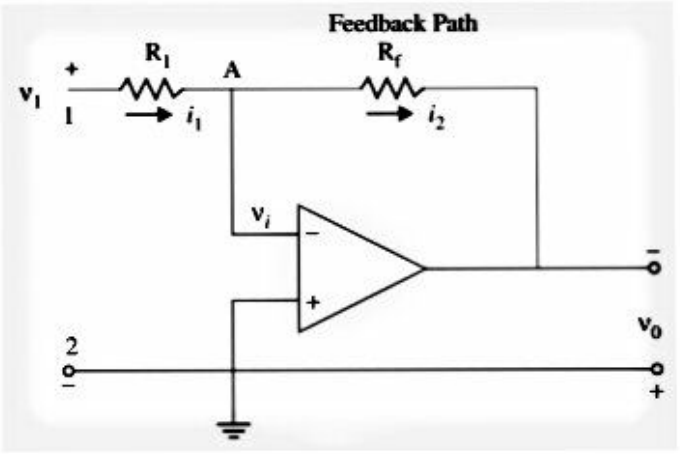


Fig. 68.4

68.6. Why V_i is Reduced to Almost Zero ?

When v_1 is applied, point *A* attains some positive potential and at the same time v_0 is brought into existence. Due to negative feedback, some fraction of the output voltage is fed back to point *A* antiphase with the voltage already existing there (due to v_1).

The algebraic sum of the two voltages is almost zero so that $v_i \cong 0$. Obviously, v_i will become exactly zero when **negative feedback voltage at A is exactly equal to the positive voltage produced by v_1 at A.**

Another point worth considering is that there exists a virtual short between the two terminals of the *OP-AMP* because $v_i = 0$. It is virtual because no current flows (remember $i = 0$) despite the existence of this short.

68.7. OP-AMP Applications

We will consider the following applications :

1. as scalar or linear (*i.e.*, small-signal) constant-gain amplifier both inverting and non-inverting,
2. as unity follower,
3. Adder or Summer
4. Subtractor,
5. Integrator
6. Differentiator
7. Comparator.

Now, we will discuss the above circuits one by one assuming an ideal *OP-AMP.*

68.8. Linear Amplifier

We will consider the functioning of an *OP-AMP* as constant-gain amplifier both in the inverting and non-inverting configurations.

(*a*) Inverting Amplifier or Negative Scale.

As shown in Fig. 68.5, noninverting

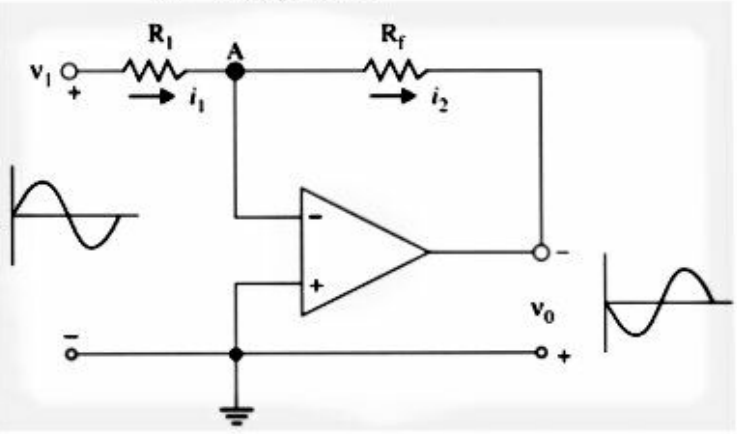


Fig. 68.5

Gain

Since point A is at ground potential*, $i_1 = \frac{v_{in}}{R_1} = \frac{v_1}{R_1}$

$$i_2 = \frac{-v_0}{R_f} \quad \text{Please note –ve sign}$$

Using *KCL* (Art. 2.2) for point A,

$$i_1 + (-i_2) = 0 \quad \text{or} \quad \frac{v_1}{R_1} + \frac{v_0}{R_f} = 0 \quad \text{or} \quad \frac{v_0}{R_f} = -\frac{v_1}{R_1} \quad \text{or} \quad \frac{v_0}{v_1} = -\frac{R_f}{R_1}$$

$$\therefore \quad A_v = -\frac{R_f}{R_1} \quad \text{or} \quad A_v = -K \quad \text{Also, } v_0 = -Kv_{in}$$

It is seen from above, that closed-loop gain of the inverting amplifier depends on the ratio of the two external resistors R_1 and R_f and is independent of the amplifier parameters.

It is also seen that the *OP-AMP* works as a negative scaler. It scales the input *i.e.*, it multiplies the input by a minus constant factor K.

(*b*) Non-inverting Amplifier or Positive Scaler

This circuit is used when there is need for an output which is equal to the input multiplied by a positive constant. Such a positive scaler circuit which uses negative feedback but provides an output that equals the input multiplied by a positive constant is shown in Fig. 68.6.

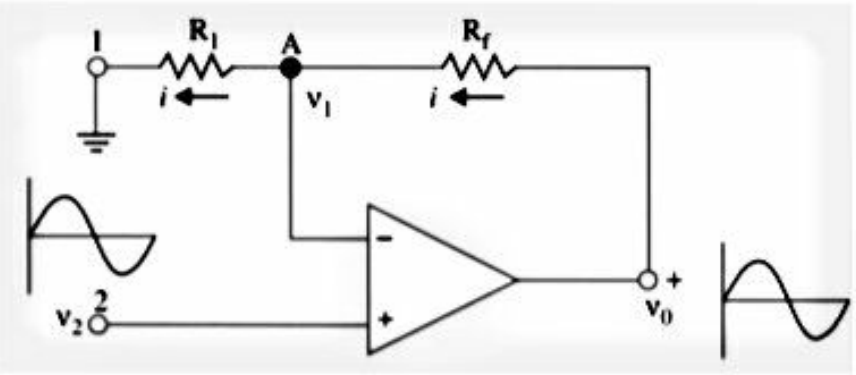


Fig. 68.6

Since input voltage v_2 is applied to the non-inverting terminal, the circuits is also called **non-inverting amplifier.**

Here, polarity of v_0 is the same as that v_2 *i.e.*, both are positive.

Gain

Because of virtual short between the two *OP-AMP* terminals, voltage across R_1 is the input voltage v_2. Also, v_0 is applied across the series combination of R_1 and R_f.

$$\therefore \quad v_{in} = v_2 = iR_1, v_0 = i(R_1 + R_f)$$

$$\therefore \quad A_v = \frac{v_0}{v_{in}} = \frac{i(R_1 + R_f)}{iR_1} \quad \text{or} \quad A_v = \frac{R_1 + R_f}{R_1} = \left(1 + \frac{R_f}{R_1}\right)$$

Alternative Derivation

As shown in Fig. 68.7, let the currents through the two resistors be i_1 and i_2.

The voltage across R_1 is v_2 and that across R_f is $(v_0 - v_2)$.

$$\therefore \quad i_1 = \frac{v_2}{R_1} \quad \text{and} \quad i_2 = \frac{v_0 - v_2}{R_f}$$

Applying *KCL* to junction A, we have

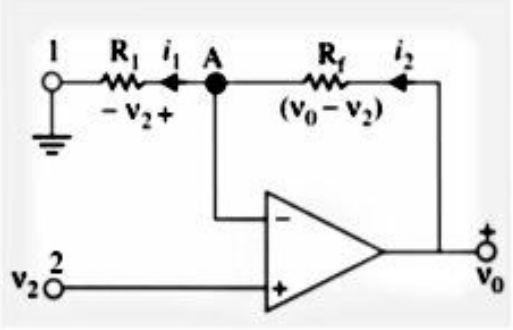


Fig. 68.7

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* If not, then $i_1 = \frac{v_1 - v_i}{R_1}$ and $i_2 = \frac{v_0 - v_1}{R_f}$

$$(-i_1) + i_2 = 0 \quad \text{or} \quad \frac{v_2}{R_1} + \frac{(v_0 - v_2)}{R_f} = 0$$

$$\therefore \quad \frac{v_0}{R_f} = v_2\left(\frac{1}{R_1} + \frac{1}{R_f}\right) = v_2\,\frac{R_1 + R_f}{R_1 R_f}$$

$$\therefore \quad \frac{v_0}{v_2} = \frac{R_1 + R_f}{R_1} \quad \text{or} \quad A_v = 1 + \frac{R_f}{R_1} \quad \text{—as before}$$

Example 68.1. *For the inverting amplifier of Fig. 68.5, R_1 = 1 K and R_f = 1 M. Assuming an ideal OP-AMP amplifier, determine the following circuit values :*

(a) voltage gain, (b) input resistance, (c) output resistance

Solution. It should be noted that we will be calculating values of the circuit and not *for* the *OP-AMP proper.*

(*a*) $$A_v = -\frac{R_f}{R_1} = -\frac{1000\ K}{1\ K} = -1000$$

(*b*) Because of virtual ground at *A*, $R_{in} = R_1 = 1\ \text{K}$

(*c*) Output resistance of the circuit equal the output resistance of the *OP-AMP i.e.*, **zero ohm.**

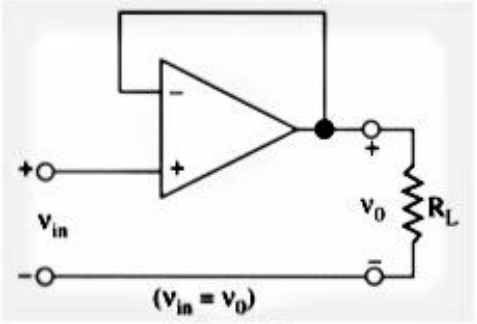

Fig. 68.8

68.9. Unity Follower

It provides a gain of unity without any phase reversal. It is very much similar to the emitter follower (Art 68.8) except that its gain is very much closer to being exactly unity.

This circuit (Fig. 68.8) is useful as a buffer or isolation amplifier because it allows, input voltage v_{in} to be transferred as output voltage v_0 while at the same time preventing load resistance R_L from loading down the input source. It is due to the fact that its $R_i = \infty$ and $R_0 = 0$.

In fact, circuit of Fig. 68.8 can be obtained from that of Fig. 68.6 by putting

$$R_1 = R_f = 0$$

68.10. Adder to Summer

The adder circuit provides an output voltage proportional to or equal to the algebraic sum of two or more input voltages each multiplied by a constant gain factor. It is basically similar to a scaler (Fig. 68.5) except that it has more than one input. Fig. 68.9 shows a three-input inverting adder circuit. As seen, ***the output voltage is phase-inverted.***

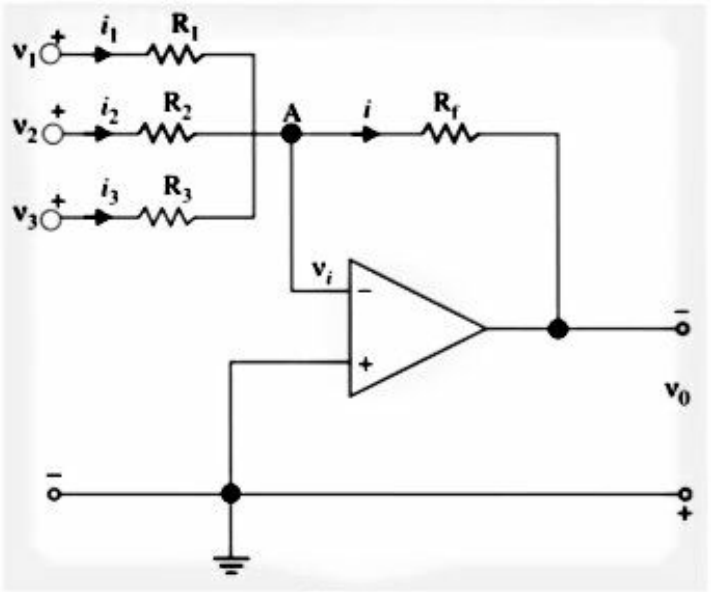

Fig. 68.9

Calculations

As before, we will treat point *A* as virtual ground

$$i_1 = \frac{v_1}{R_1} \quad \text{and} \quad i_2 = \frac{v_2}{R_2}$$

$$i_3 = \frac{v_3}{R_3} \quad \text{and} \quad i = -\frac{v_0}{R_f}$$

Applying *KCI* to point *A*, we have

$$i_1 + i_2 + i_3 + (-i) = 0$$

or $$\frac{v_1}{R_1}+\frac{v_2}{R_2}+\frac{v_3}{R_3}-\left(\frac{-v_0}{R_f}\right)=0$$

$$\therefore \quad v_0=-\left(\frac{R_f}{R_1}v_1+\frac{R_f}{R_2}v_2+\frac{R_f}{R_3}v_3\right)$$

or $$v_0=-(K_1v_1+K_2v_2+K_3v_3)$$

The overall negative sign is unavoidable because we are using the inverting input terminal.

If $R_1 = R_2 = R_3 = R$, then

$$v_0 = -\frac{R_f}{R}(v_1+v_2+v_3) = -K(v_1+v_2+v_3)$$

Hence, output voltage is proportional to (*not equal to*) the **algebraic sum** of the three input voltages.

If $R_f = R$, then ouput exactly equals the sum of inputs. However, if $R_f = R/3$

then $$v_0 = -\frac{R/3}{R}(v_1+v_2+v_3) = -\frac{1}{3}(v_1+v_2+v_3)$$

Obviously, the output is equal ***to the average of the three inputs.***

68.11. Subtractor

The function of a subtractor is to provide an output proportional to or equal to the difference of two input signals. As shown in Fig. 68.10 we have to apply the inputs at the inverting as well as non-inverting terminals.

Calculations

According to Superposition Theorem (Art. 2.17) $v_0 = v_0' + v_0''$

where v_0' is the output produced by v_1 and v_0'' is that produced by v_2.

Now, $$v_0' = -\frac{R_f}{R_1}\cdot v_1 \qquad \text{...Art 67.37 } (a)$$

$$v_0'' = \left(1+\frac{R_f}{R_1}\right)v_2 \qquad \text{...Art 67.37 } (b)$$

$$\therefore \quad v_0 = \left(1+\frac{R_f}{R_1}\right)v_2 - \frac{R_f}{R_1}\cdot v_1$$

Since $R_f \gg R_1$ and $R_f/R_1 \gg 1$, hence

$$v_0 \cong \frac{R_f}{R_1}(v_2-v_1) = K(v_2-v_1)$$

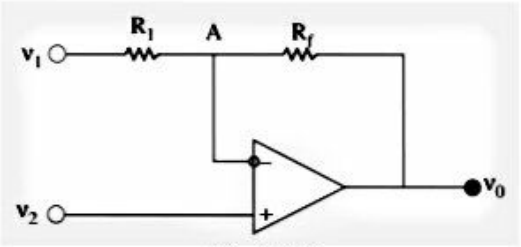

Fig. 68.10

Further, If $R_f = R_1$, then

$$v_0 = (v_2-v_1) = \text{difference of the two input voltages}$$

Obviously, if $R_f \neq R_1$, then a scale factor is introduced.

Example 68.2. *Find the output voltages of an OP-AMP inverting adder for the following sets of input voltages and resistors. In all cases, R_f = 1 M.*

$$v_1 = -3\,V, v_2 = +3V, v_3 = +2V; R_1 = 250\,K, R_2 = 500\,K, R_3 = 1\,M$$

[Electronic Engg. Nagpur Univ. 1991]

Solution. $$v_0 = -(K_1v_1+K_2v_2+K_3v_3)$$

$$K_1 = \frac{R_f}{R_1} = \frac{1000\,K}{250\,K} = 4,\ K_2 = \frac{1000}{500} = 2,\ K_3 = \frac{1M}{1M} = 1$$

$$\therefore \quad v_0 = -[(4 \times -3) + (2 \times 3) + (1 \times 2)] = +4\text{V}$$

Example 68.3. *In the subtractor circuit of Fig. 68.10, $R_1 = 5$ K, $R_f = 10$ K, $v_1 = 4$ V and $v_2 = 5$ V. Find the value of output voltage.*

Solution. $$v_0 = \left(1 + \frac{R_f}{R_1}\right) v_1 - \frac{R_f}{R_1} v_2 = \left(1 + \frac{10}{5}\right) 4 - \frac{10}{5} \times 5 = +2\text{V}$$

Example 68.4. *Design an OP-AMP circuit that will produce an output equal to $-(4\, v_1 + v_2 + 0{\cdot}1\, v_3)$. Write an expression for the output and sketch its output waveform when $v_1 = 2 \sin \omega t$, $v_2 = +5$ V dc and $v_3 = -100$ V dc.* **[Banglore University 2001]**

Solution. $$v_0 = -\left[\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3\right] \quad \ldots(1)$$

and also $$v_0 = -(4 v_1 + v_2 + 0{\cdot}1\, v_3) \quad \ldots(2)$$

Comparing equations (1) and (2), we find,

$$\frac{R_f}{R_1} = 4, \quad \frac{R_f}{R_2} = 1, \quad \frac{R_f}{R_3} = 0{\cdot}1$$

Therefore if we assume $R_f = 100\ K$, then $R_1 = 25\ K$, $R_2 = 100\ K$ and $R_3 = 10\ K$. With there values of R_1, R_2 and R_3, the *OP-AMP* circuit is as shown in Fig. 68.11(*a*)

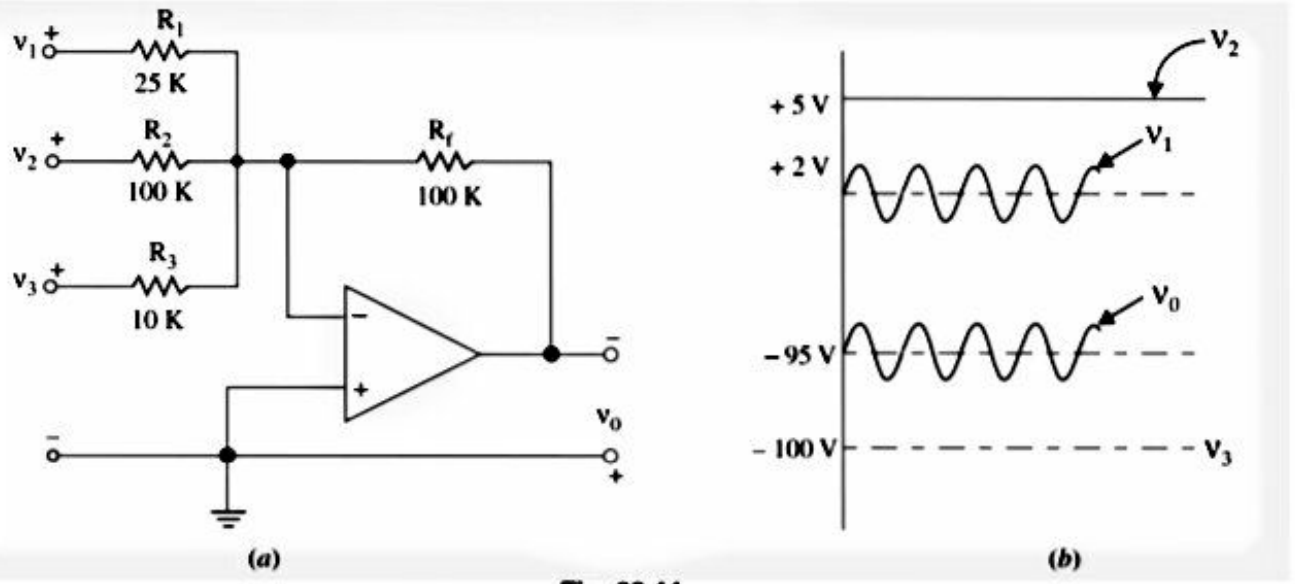

Fig. 68.11

With the given values of $v_1 = 2 \sin \omega t$, $v_2 = +5$V, $v_3 = -100$ V dc, the output voltage, $v_0 = 2 \sin \omega t + 5 - 100 = 2 \sin \omega t - 95$ V. The waveform of the output voltage is sketched as shown in Fig. 68.11 (*b*).

68.12. Integrator

The function of an integrator is to provide an output voltage which is proportional to the integral of the input voltage.

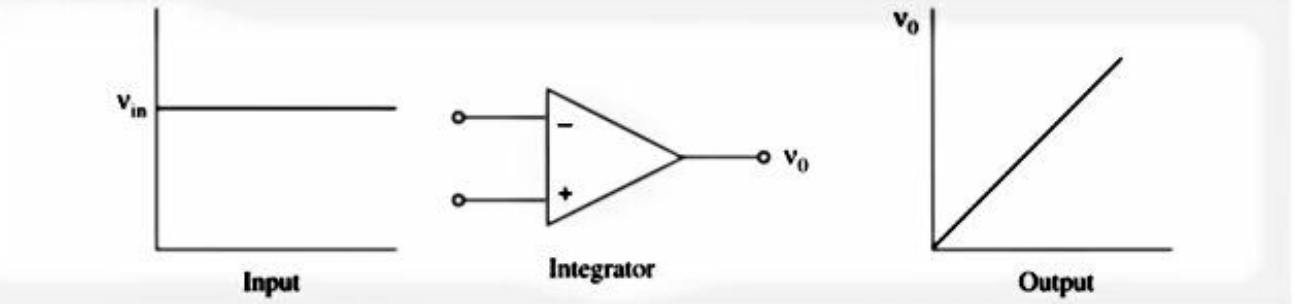

Fig. 68.12

A simple example of integration is shown in Fig. 68.12 where input is dc level and its integral is *a linearly-increasing ramp output.* The actual integration circuit is shown in Fig. 68.13. This circuit is similar to the scaler circuit of Fig. 68.5 except that **the feedback component is a capacitor C instead of a resistor R_f.**

Calculations

As before, point *A* will be treated as virtual ground.

$$i_1 = \frac{v_1}{R} \; ; i_2 = -\frac{v_0}{X_C} = -\frac{v_0}{1/j\omega C} = -\frac{v_0}{1/sC} = -sC v_0$$

where $s = j\omega$ in the Laplace notation.

Now $i_1 = i_2$ ...Art. 68.26 (*a*)

$$\therefore \quad \frac{v_1}{R} = -sCv_0$$

$$\therefore \quad \frac{v_0}{v_{in}} = \frac{v_0}{v_1} = -\frac{1}{sCR} \qquad ...(i)$$

$$\therefore \quad A_v = -\frac{1}{sCR}$$

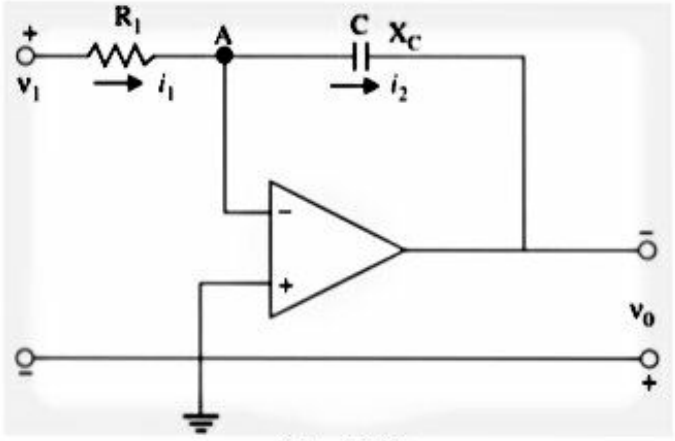

Fig. 68.13

Now, the expression of Eq. (*i*) can be written in time domain as

$$v_0(t) = -\frac{1}{40\pi}(\cos 2000\pi t - 1)$$

It is seen from above that output (right-hand side expression) is an integral of the input, with an inversion and a scale factor of $1/CR$.

This ability to integrate a given signal enables an analog computer solve differential equations and to set up a wide variety of electrical circuit analogs of physical system operation. For example, let

$$R = 1\,\text{M} \quad \text{and} \quad C = 1\,\mu\text{F}. \text{ Then}$$

$$\text{scale factor} = -\frac{1}{CR} = -\frac{1}{10^6 \times 10^{-6}} = -1$$

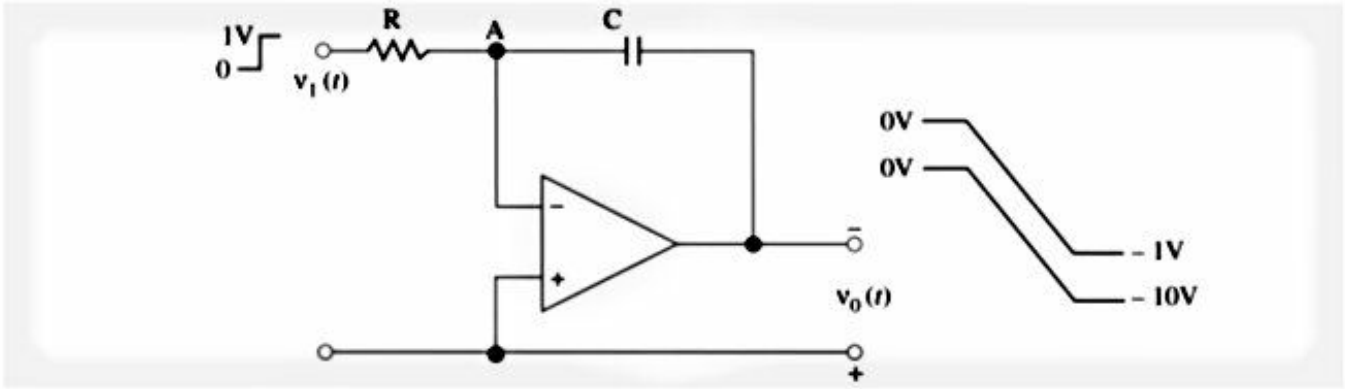

Fig. 68.14

As shown in Fig. 68.14 the input is a step voltage, whereas output is a ramp (or linearly-changing voltages) with a scale multiplier of −1. However, when R = 100 K, then

$$\text{scale factor} = -\frac{1}{10^5 \times 10^{-6}} = -10$$

$$\therefore \quad v_0(t) = -10\int v_1(t)\,.\,dt$$

It is also shown in Fig. 68.14. Of course, we can integrate more than one input as shown below in Fig. 68.15. With multiple inputs, the output is given by

68.13. Differentiator

Its function is to provide an output voltage which is ***proportional to the rate of the change of the input voltage.*** It is an inverse mathematical operation to that of an integrator. As shown in Fig. 68.16, when we feed a differentiator with linearly-increasing ramp input, we get a constant dc output.

Circuit

Differentiator circuit can be obtained by interchanging the resistor and capacitor of the integrator circuit of Fig. 68.13.

Let i = rate of change of charge $= \frac{dq}{dt}$

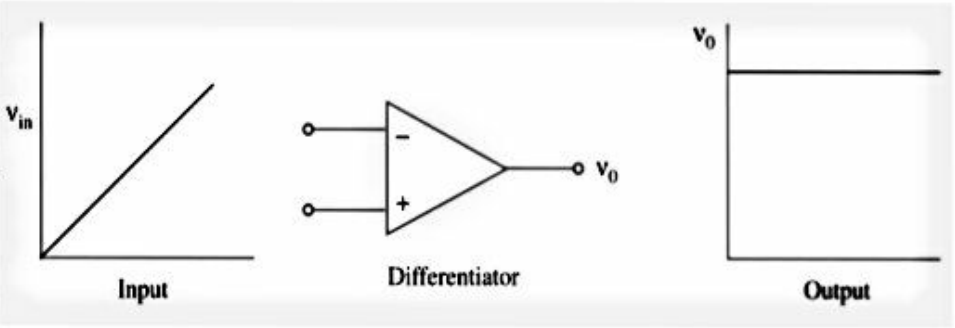

Fig. 68.16

Now, $q = Cv_c$

$$\therefore \quad i = \frac{d}{dt}(Cv_c) = C\frac{dv_c}{dt}$$

Taking point A as virtual ground

$$v_0 = -iR = -\left(C \cdot \frac{dv_c}{dt}\right)R = -CR \cdot \frac{dv_c}{dt}$$

As seen, output voltage is proportional to the derivate of the input voltage, the constant of proportionality (*i.e.*, scale factor) being $(-RC)$.

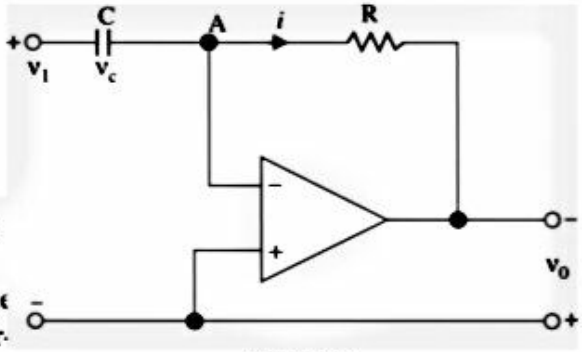

Fig. 68.17

Example 68.6. *The input to the differentiator circuit of Fig. 68.17 is a sinusoidal voltage of peak value of 5 mV and frequency 1 kHz. Find out the output if R = 1000 K and C = 1 μF.*

Solution. The equation of the input voltage is

$$v_1 = 5 \sin 2\pi \times 1000\, t = 5 \sin 2000\, \pi t \text{ mV}$$

scale factor $= CR = 10^{-6} \times 10^5 = 0{\cdot}1$

$$v_0 = 0{\cdot}1 \frac{d}{dt}(5 \sin 2000\, \pi t) = (0{\cdot}5 \times 2000\, \pi) \cos 2000\, \pi t = 1000\, \pi \cos 2000\, \pi t \text{ mV}$$

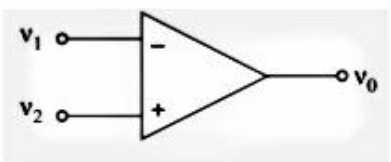

Fig. 68.18

As seen, output is a cosinusoidal voltage of frequency 1 kHz

(i) Slew Rate :

One of the important frequency related parameter of an op-amp is the slew rate. The slew rate is the maximum rate of change of output voltage caused by a step input voltage and is usually specified in V/μS. For example 1V/μS slew rate means that the output rises or falls by 1V in one microseconds. Ideally slew rate is infinite which means that op-amp's output should be changed instantaneously in response to input step voltage. Practical op-amp are available with slew rates from 0.1V/μS to well above 1000V/μS.

(ii) CMRR :

Common Mode Rejection Ratio is defined in several essentially equivalent ways by the various manufacturers. Generally, it can be defined as the ratio of the differential gain AD to the common mode gain A_{CM} that is,

$$CMRR = \frac{A_D}{A_{CM}}$$

For 741C, CMRR is typically 90dB. CMRR is usually expressed under the test condition that the input source resistance $R_S \leq 10k\Omega$. Higher the value of CMRR, better is the matching between two input terminals and smaller the output common-mode voltage.

(iii) Input offset voltage :

Input offset voltage V_io is the differential input voltage that exists between two input terminals of an op-amp without any external inputs applied. In other words, it is the amount of the input voltage that should be applied between two input terminals in order to force the output voltage to zero. Since this voltage could be positive or negative its absolute value is listed on the data sheet. For 741C, the maximum value is 6mV.

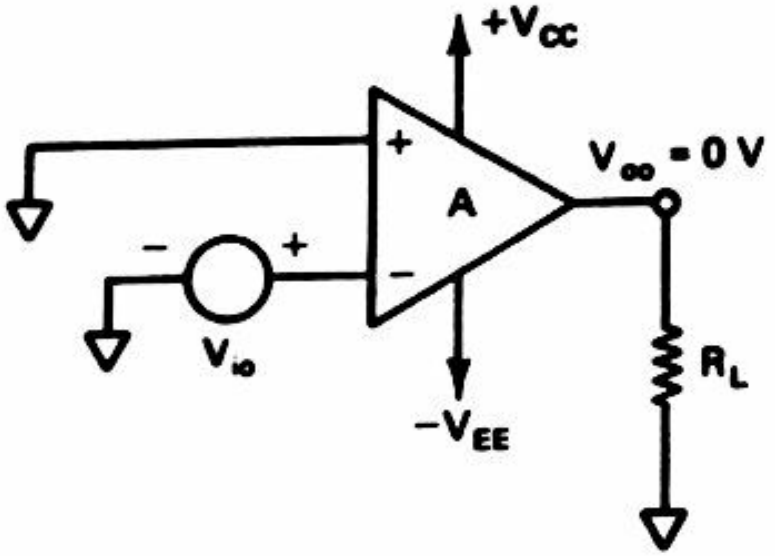

Figure 1: Input Offset Voltage in op-amp

(iv) Output offset voltage :

- The output offset voltage VOO is caused by mismatching between two input terminals. Even though all the components are integrated on the same chip, it is not possible to have two transistors in the input differential amplifier stage with exactly the same characteristics.
- This means that the collector currents in these two transistors are not equal, which causes a differential output voltage from the first stage.
- The output of first stage is amplified by following stages and possibly aggravated by more mismatching in them. Thus output voltage caused by mismatching between two input terminals is the output offset V_{OO}.
- The output offset voltage is a dc voltage; it may be positive or negative in polarity depending on whether the potential difference between two input terminals is positive or negative.

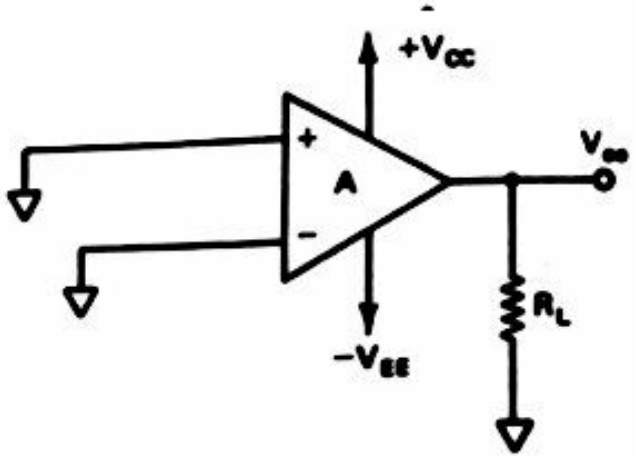

Figure 2 : Output offset voltage in op-amp

(v) PSRR :

The change in an op-amp's input offset voltage due to variations in supply voltage is called as power supply rejection ratio (PSRR) or called as supply voltage rejection ratio (SVRR). This term is expressed in microvolts per volt or decibels. For 741C, PSRR=150μV/V, lower the value of PSRR, better the op-amps.